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THESIS

SOLID STATE CAPACITOR DISCHARGE PULSED POWER SUPPLY DESIGN FOR RAILGUNS

by

Jesse H. Black

March 2007

Thesis Advisor: Alexander L. Julian
Co-Advisor: William B. Maier II

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY ***(Leave blank)***	**2. REPORT DATE** March 2007	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE Solid State Capacitor Discharge Pulsed Power Supply Design for Railguns.		**5. FUNDING NUMBERS**	
6. AUTHOR(S) Jesse H. Black			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000		**8. PERFORMING ORGANIZATION REPORT NUMBER**	
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A		**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**	
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited.		**12b. DISTRIBUTION CODE** A	

13. ABSTRACT (maximum 200 words)

This thesis presents a solid state thyristor switched power supply capable of providing 50 kJ from a high voltage capacitor to a railgun. The efficiency with which energy is transferred from a power supply to a projectile depends strongly on power supply characteristics. This design will provide a better impedance match to the railgun than power supplies utilizing spark gap switches. This supply will cost less and take up less volume than a similar supply using spark gap switches; it will also produce a smaller electromagnetic pulse. Voltage limitations on the thyristors require two in series acting as a single switch. Railgun, snubber circuit and gate control systems were modeled for a 50 kJ railgun supply. These simulations yielded component values necessary to protect and control the thyristors for voltages up to 10 kV, currents up to 180 kA, and changes in current with respect to time up to 10^9 A/s.

14. SUBJECT TERMS Pulsed Power, Thyristor, Gate Control Circuit, Snubber Circuit.			**15. NUMBER OF PAGES** 74
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UL

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

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SOLID STATE CAPACITOR DISCHARGE PULSED POWER SUPPLY FOR RAILGUNS

Jesse H. Black
Lieutenant, United States Navy
B.S., University of Idaho, 2000

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 2007

Author: Jesse H. Black

Approved by: Alexander L. Julian
Thesis Advisor

William B. Maier II
Co-Advisor

Jeffery B. Knorr
Chairman, Department of Electrical Engineering

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ABSTRACT

This thesis presents a solid state thyristor switched power supply capable of providing 50 kJ from a high voltage capacitor to a railgun. The efficiency with which energy is transferred from a power supply to a projectile depends strongly on power supply characteristics. This design will provide a better impedance match to the railgun than power supplies utilizing spark gap switches. This supply will cost less and take up less volume than a similar supply using spark gap switches; it will also produce a smaller electromagnetic pulse. Voltage limitations on the thyristors require two in series acting as a single switch. Railgun, snubber circuit and gate control systems were modeled for a 50 kJ railgun supply. These simulations yielded component values necessary to protect and control the thyristors for voltages up to 10 kV, currents up to 180 kA, and changes in current with respect to time up to 10^9 A/s.

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ACKNOWLEDGMENTS

I would like to start by thanking my advisors, Professor Alex Julian and Professor Bill Maier for their guidance in this thesis research. I would like to thank my parents, my brothers, and my sisters for the love and support they have given me. Thanks for being interested in the things I do. Finally and most importantly, I would like to thank my wife Kristi, my daughter Megan and my son Josh. You give me purpose.

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I. INTRODUCTION

A. PURPOSE

The purpose of this thesis was to design a Solid State power supply for ongoing research in the Naval Postgraduate School's Railgun program. Currently the power supplies use "Titan High-Action Spark Gap Switches" to transfer energy from high voltage electrolytic capacitors to a large inductor for current pulse shaping and then onto the Railgun. Although these power supplies and switches have proven to be reliable, there is a need for them to be improved. A solid state design using thyristors (also known as Silicon Controlled Rectifiers (SCRs)) will be more efficient, cost less and take up less volume due to design simplification. The physical construction of the switches will also reduce the electromagnetic signature. Finally, this design is important because the Navy's railgun power supplies will be switched this way in the future [1].

Two top level concerns will be addressed in this thesis. First, companies that build these parts provide data sheets with listed limitations. The problem is that industry does not make these large thyristors for impulse power applications. They are made to be used by industry in continuous power applications. This design will begin to explore how to use the thyristors in railguns and not break them. The second concern addressed in the design is preventing false or intermittent triggering of the thyristors. It is paramount to have full control of when the thyristors trigger at the large energy and power levels appropriate for railguns.

B. OVERVIEW

The Mission of the Electromagnetic Railgun (EMRG) Innovative Naval Program, based out of the Office of Naval Research (ONR), is to develop the science and technology (S&T) necessary to design, test, and install a revolutionary 64 Mega Joule (MJ) EMRG aboard United States (U.S.) Navy Ships in the 2020-2025 timeframe [2]. In the fall of 2006 the Navy commissioned an 8 MJ Railgun at the Electromagnetic Launch

Facility (EMLF) at Naval Surface Warfare Center (NSWC), Dahlgren, VA. By the summer of 2007 NSWC will have a 32 MJ railgun delivered and the program schedule has it fully operational by 2009.

There are many advantages to changing to this type of weapon over a standard gun. From the logistics and storage perspective these rounds are non-explosive. This means a large reduction in logistical cost. Also, the magazine can be reduced in size because it is considered non-explosive and it does not have to be designed to withstand damage or prevent high explosive inadvertent discharge. Figure 1 shows the other benefits of the Railgun as compared to the ERGM and LRAP rounds. A smaller projectile delivers more energy to the target, at a further distance in a shorter period of time. The energy on target is defined as Kinetic Energy computed from summing the quantity of fragments and average impact velocity. Under each round in Figure 1 the weight is shown with two numbers. The first number is the weight of the projectile itself and the second number is the weight of the propellant charge. The railgun round, which does not use a propellant charge, lists the equivalent amount of fuel. Two other benefits include the ability to scale up and/or down the weapon system and less recoil exerted on the mount [3].

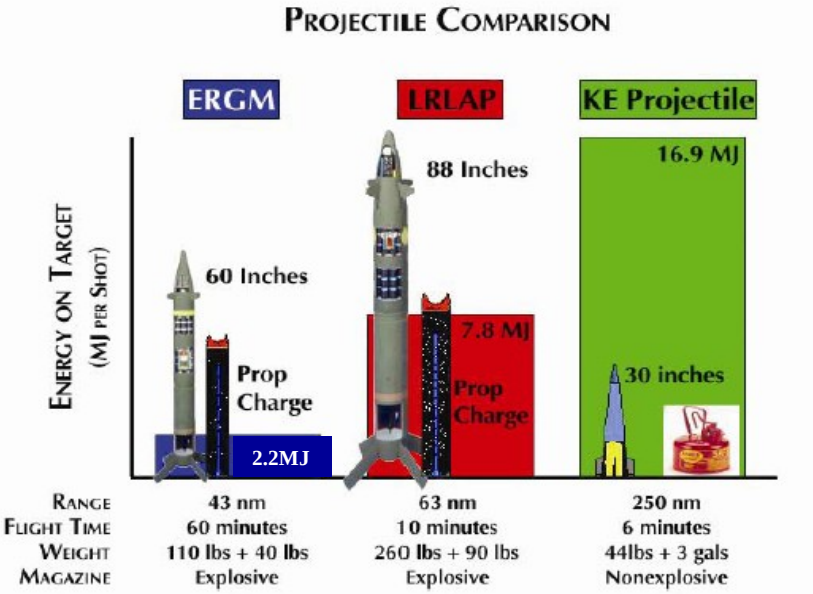

Figure 1. Projectile Comparison [from Ref.4].

Not until the past couple of years have other institutions within the Railgun community made promising improvements; however, there are still significant technical issues that need to be resolved in order to sustain the program. The railgun is made up of subsystems which include the power supply, the gun, and the projectile. For the power supply the major concerns are the energy storage elements, and what the switching typology will be. For the gun they include reducing the size of the system, increasing bore life and reducing EMP. Finally the projectile has to withstand the incredible amount of force, acceleration and EMP exerted upon it. If improvements are not made in all three subsystems, the total system has the chance of being terminated.

C. APPROACH / THESIS ORGANIZATION

The new power supply was designed from the perspective of system as a whole. Subsystems for detail circuits and major components were then identified. Component behavior was modeled by solving mathematical equations in Simulink, a software subprogram that runs inside Matlab. The model yielded limitations from which component selection was made. Besides the thyristors, diodes and inductor the power supply also has two separate sub-circuits that needed to be designed. A snubber circuit was designed to protect the thyristors statically and dynamically. Then a gate control circuit was designed to ignite the thyristors. Each of these two sub-circuits were put onto Printed Circuit Boards (PCB) that were designed and laid out with an online software tool called PCB123. Once the boards were populated the system was then put into Rhino a 3-D CAD software tool for final component placement and bussing dimensioning.

Chapter II will detail the design for the entire power supply. Chapter III will detail the results from the testing of the gate control circuit and Chapter IV will highlight future and follow on work.

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II. DESIGN

A. POWER SUPPLY

1. Introduction

The starting point of this design centered on the capacitor and its specifications. The railgun lab currently has six 11 kV, 50 kJ, 0.83 mf capacitors waiting to be placed in power supplies. The design focused on a single capacitor per supply with the intent to increase to two capacitors in parallel. Two capacitors would supply 100 kJ which is equivalent to the other two supplies currently in operation. Figure 2 shows the electric circuit. Once the capacitors are charged up to firing voltage, the two thyristors are triggered and forced into forward conduction mode. Energy is then transferred to from the capacitor to the inductor through the railgun. The crowbar diodes then go into forward conduction and the rest of the energy is then released into the railgun.

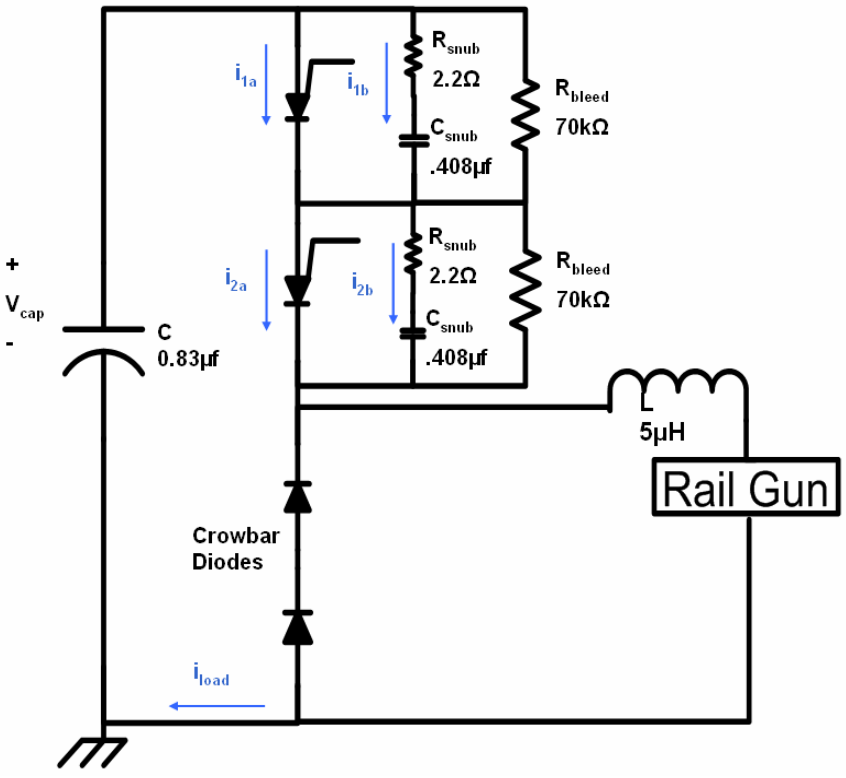

Figure 2. Electric Circuit.

2. Model Simulation Using Simulink and Matlab

The railgun model presented here was used to approximate the shape of the source current and quantify the voltage stress on the circuit components [4].

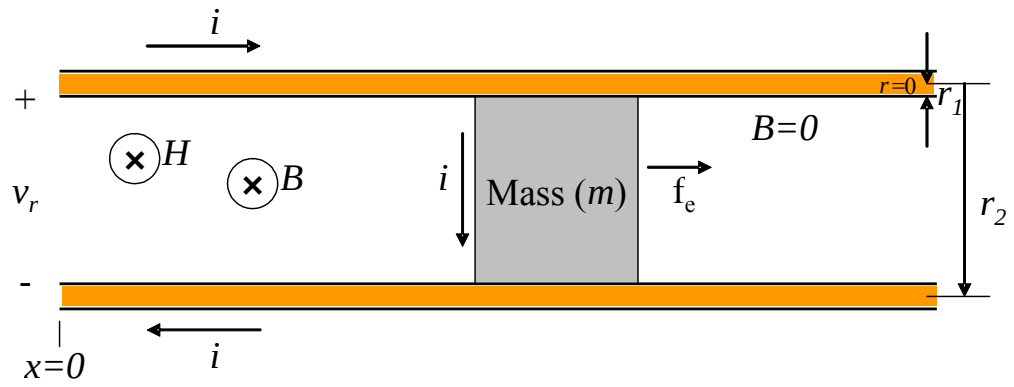

Figure 3. Railgun model.

The magnetic field intensity, $\vec{H}$, created by the current in the top rail, i, is a function of the distance from the center of the rail ($r = 0$):

$$\int \vec{H} \cdot d\vec{l} = i \Rightarrow H 2\pi r = i \Rightarrow H(r) = \frac{i}{2\pi r} \text{ where } r_1 > r > r_2$$

The contribution to flux linkage from the top rail is:

$$\lambda = \Phi = \int \vec{B} \cdot d\vec{S} = x \frac{\mu i}{2\pi} \int_{r_1}^{r_2} \frac{1}{r} dr = x \frac{\mu i}{2\pi} \left(\ln(r_2) - \ln(r_1) \right)$$

By symmetry the contribution to flux linkage for the bottom rail is the same. The inductance is defined as the ratio of flux linkage to current:

$$\frac{\lambda}{i} = L(x) = x \frac{\mu}{\pi} \left(\ln(r_2) - \ln(r_1) \right)$$

The railgun voltage, v_r, is:

$$v_r = \frac{d\lambda}{dt} = \frac{\mu}{\pi} \left(\ln(r_2) - \ln(r_1) \right) \left[i \frac{dx}{dt} + x \frac{di}{dt} \right] = k \left[i \frac{dx}{dt} + x \frac{di}{dt} \right]$$

$$\text{where } k = \frac{\mu}{\pi} \left(\ln(r_2) - \ln(r_1) \right)$$

For this linear magnetic circuit the coenergy stored in the coupling field is:

$$W_c = \frac{1}{2} L(x) i^2$$

The electric force acting on the mass is [5]:

$$f_e = \frac{\partial W_c}{\partial x} = \frac{\mu i^2}{2\pi}\left(\ln(r_2) - \ln(r_1)\right) = \frac{k i^2}{2}$$

The equivalent circuit to describe the power supply behavior is:

$$V_c = L\frac{di}{dt} + Ri + v_r = L\frac{di}{dt} + Ri + k\left[i\frac{dx}{dt} + x\frac{di}{dt} \right]$$

$$V_c = L\frac{di}{dt} + Ri + kiv + kx\frac{di}{dt}$$ where the velocity is $v = \frac{dx}{dt}$ and L is the circuit inductance

The rail resistance, $R(x)$, does depend on the position *x* of the mass in the railgun. The differential equation for the current is:

$$\frac{di}{dt} = \frac{V_c - Ri - kiv}{L + kx}$$ where R is the circit resistance

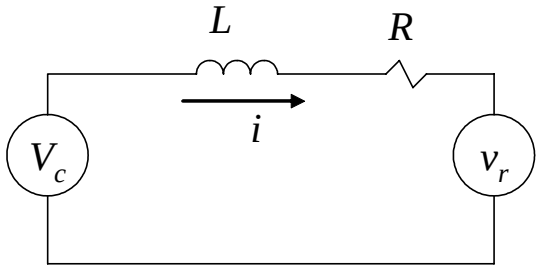

Figure 4. Electrical circuit model

The differential equations to describe the electromechanical system are:

$$\frac{dx}{dt} = v \qquad \frac{dv}{dt} = \frac{d^2x}{dt^2} = a = \frac{f_e}{m} \qquad \frac{di}{dt} = \frac{V_c - Ri - kiv}{L + kx}$$

The above equations were then programmed into Simulink and a model was developed to verify characteristic output curves for time based current and voltage.

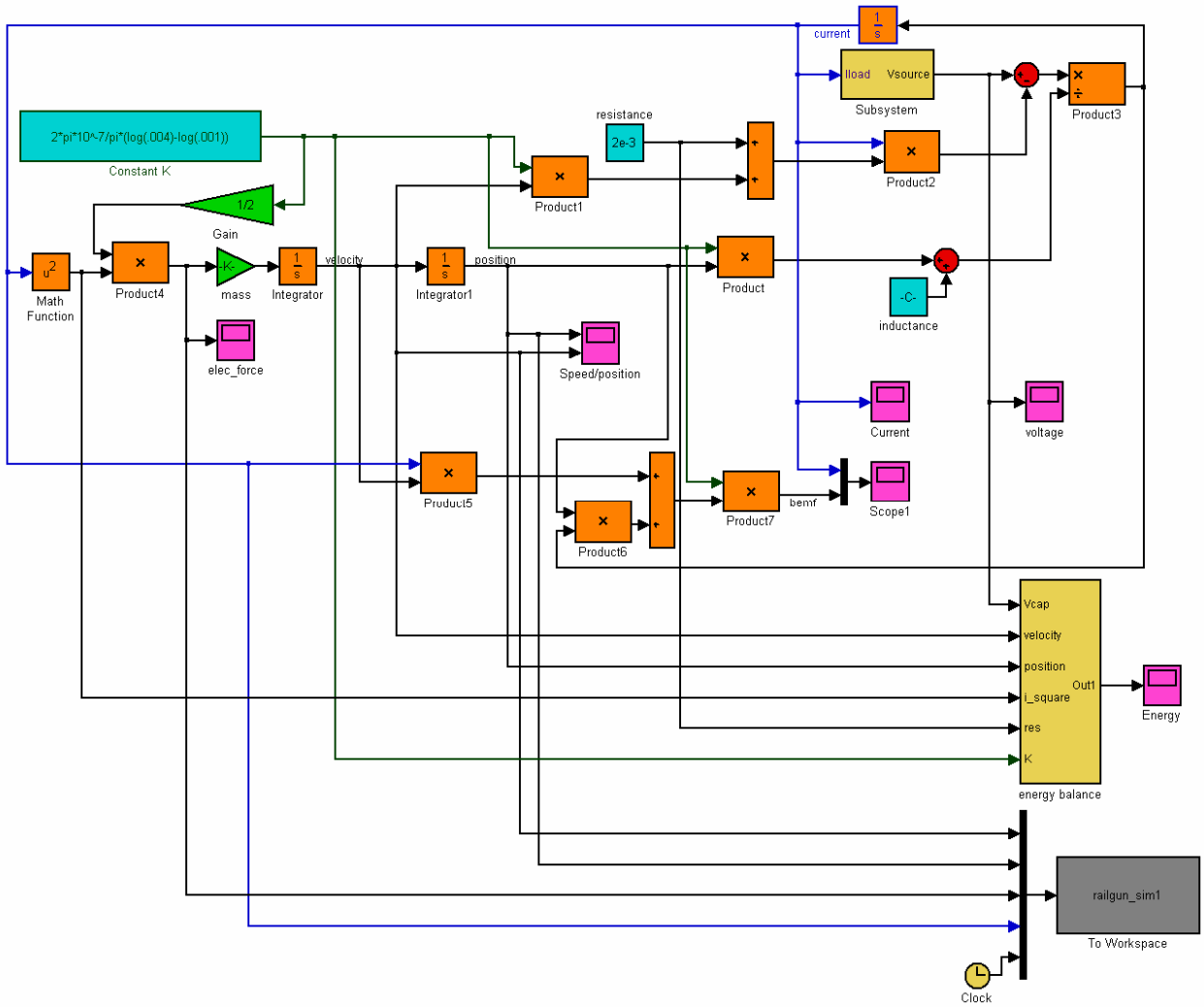

Figure 5. Simulink Model of a Railgun [from Ref 4].

3. Component Selection

Details on the snubber circuit and Gate control circuit are in sections II.B and II.C. In order to hold off the maximum voltage of the capacitor, two thyristors are placed in series, as shown in Figure 2, so that the maximum voltage across a thyristor during the hold off condition will be 5000 V. Figure 6 gives the specified maximum hold off voltage of these thyristors to be 6500 V_{DSM} [6]. The data sheet also specifies the maximum current to be 71.4 kA; however, ABB has calculated maximum sustainable currents greater or equal to 180 kA for pulses shorter than 3 ms, as shown in Figure 7. In

order to control the current rise with respect to time a minimum of $4\,\mu H$ inductor is needed. Specified maximum turn-on dI/dt to these thyristors is 1×10^{9} A/s. For a high quality factor tank circuit:

$$\frac{dI}{dt}\approx\frac{CV_0}{(\pi\sqrt{LC}/2)^2}=\frac{4V_0}{\pi^2L}$$

where C ≡ capacitance(8.3×10^{-4} F)

L ≡ Circuit Inductance (H) and V_0 is the inital charge on C.

If $V=10^4$, then $L^3\ \frac{4(10^4)}{\pi^2 10^9}=4\times10^{-6}$H.

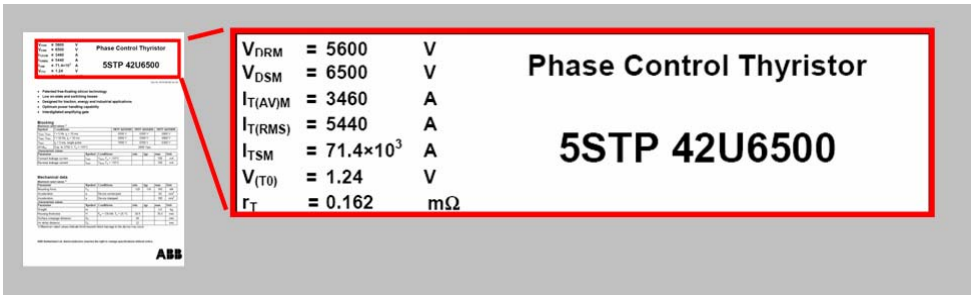

Figure 6. ABB Data Sheet for the 5STP 42U6500 Phase Control Thyristor [from Ref 6].

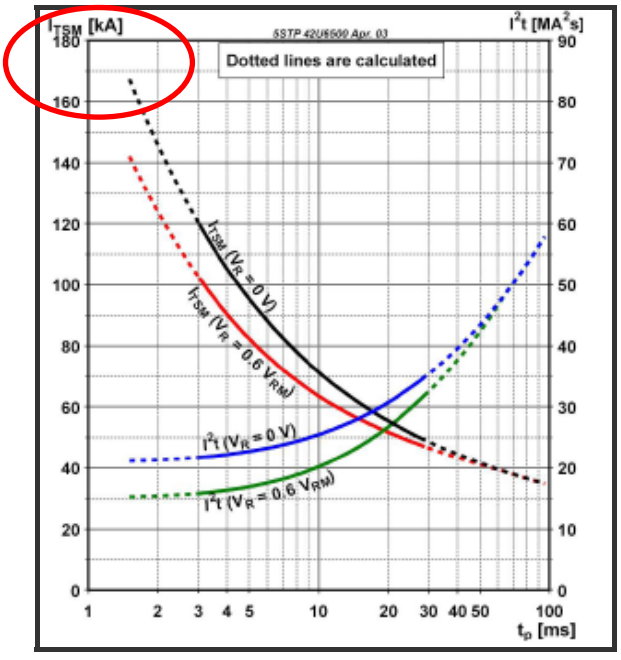

Figure 7. Surge on-state current vs. pulse length. Half-Sine wave. [from Ref 6].

4. Summary

This model of the electromechanical behavior of a railgun was developed to predict the electrical stress on a solid state switching power supply. From this model component selections were made and detailed sub-circuits were further developed.

Simulation results shown in Figures 8 and 9 were consistent with laboratory data.

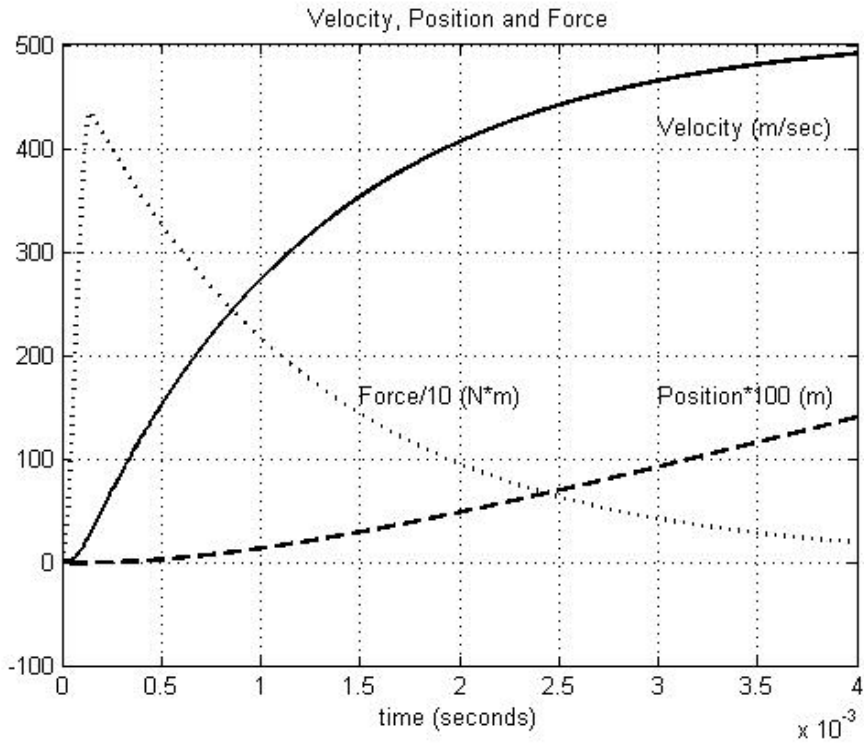

Figure 8. Simulated behavior of mechanical variables

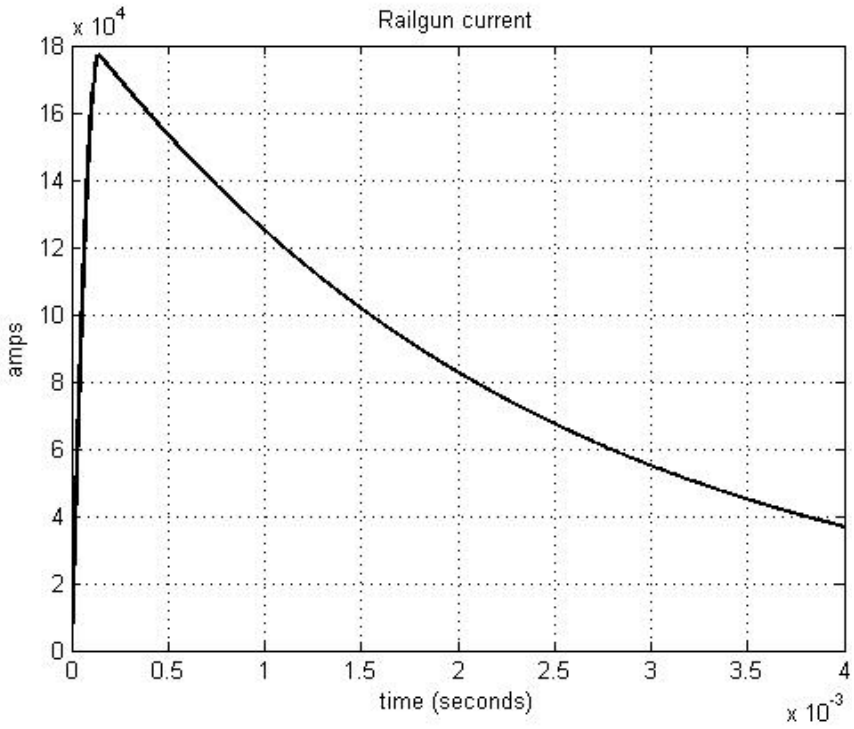

Figure 9. Simulated railgun current

B. SNUBBER CIRCUIT

1. Introduction

The snubber circuit is designed for two separate states of operation. The first state is considered the static condition and it is the point at which the thyristors are holding off the charged capacitor. Due to manufacturing tolerances each thyristor will have a slightly different leakage current. Thus, the thyristors will not share the voltage evenly. Placing a bleed resistor in parallel with one thyristor develops a voltage potential. Repeating this on the second thyristor with an equal resistor ensures that each device is at the same voltage and therefore the static load is equivalent.

The second state of operation for the snubber circuit is the dynamic state. This state is defined as the point in which one thyristor has been triggered; however, the second thyristor has not. During this time the Resistive-Capacitive (RC) portion of the snubber circuit, which has also been placed in parallel with the thyristor, will resist the

change in voltage and hold the voltage potential on the non-triggered device for a brief moment. During the delay the second thyristor will be triggered and thereby release the energy from the capacitor into the inductor.

2. Model Simulation Using Matlab

Figure 10 is a subsystem inside the Power Supply Model simulation.

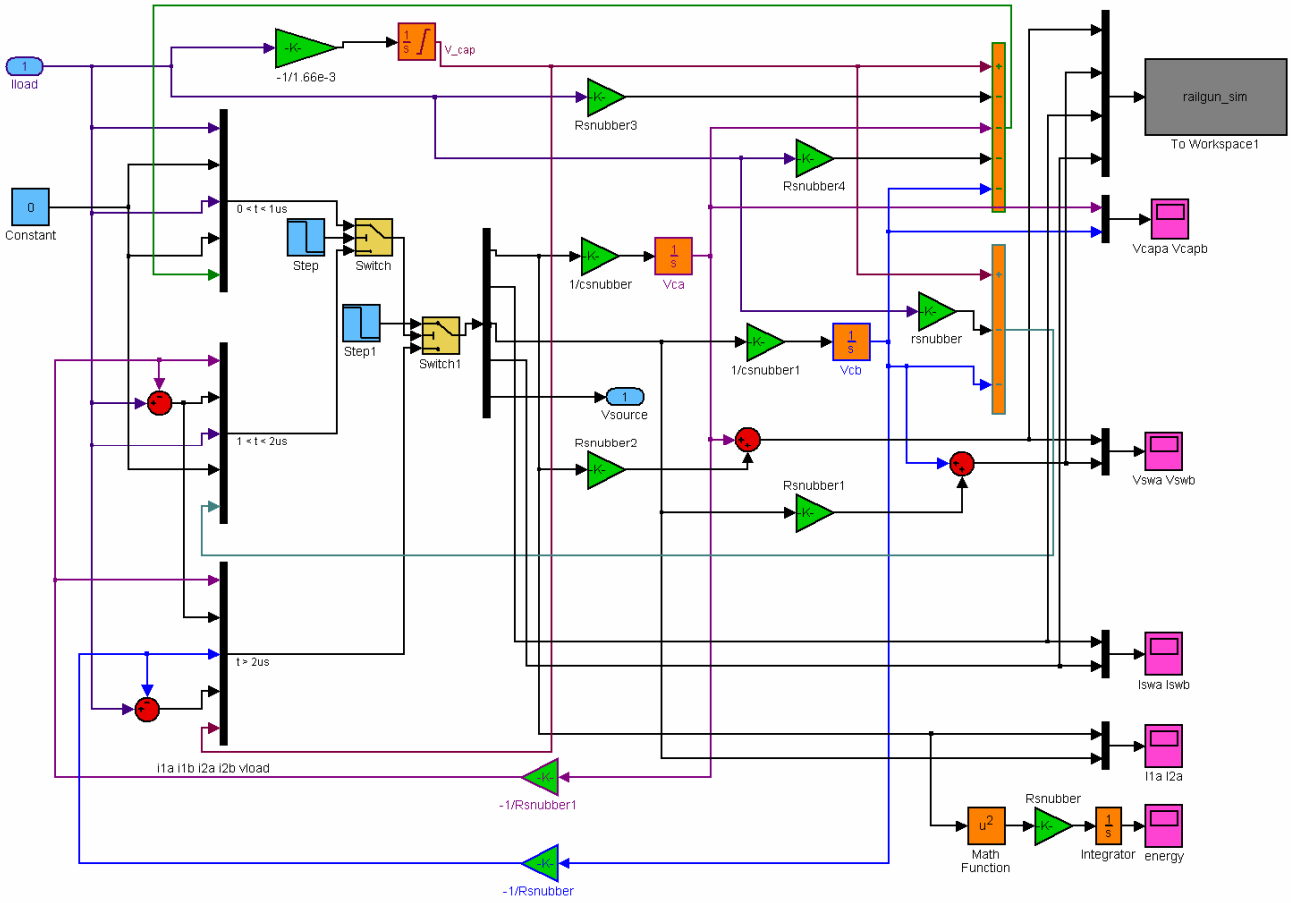

Figure 10. Simulink Model for Snubber Circuit Component selection [from Ref 4].

3. Component Selection

The following component values were input into the simulation above to obtain Figure 11. To ensure each thyristor shares the same voltage in the static condition fifteen 1 MΩ resistors were placed in parallel to make an equivalent 70 kΩ resistor. To ensure the max voltage on second thyristor does not exceed the 6500 kV limit during the

dynamic condition, six 6000 V , 0.068 μf film capacitors were placed in parallel to make an 0.408 μf equivalent capacitor. These capacitors were placed in series with four 2.2 Ω resistors. PCB123 was used to make the PCBs and is shown in Figure 11.

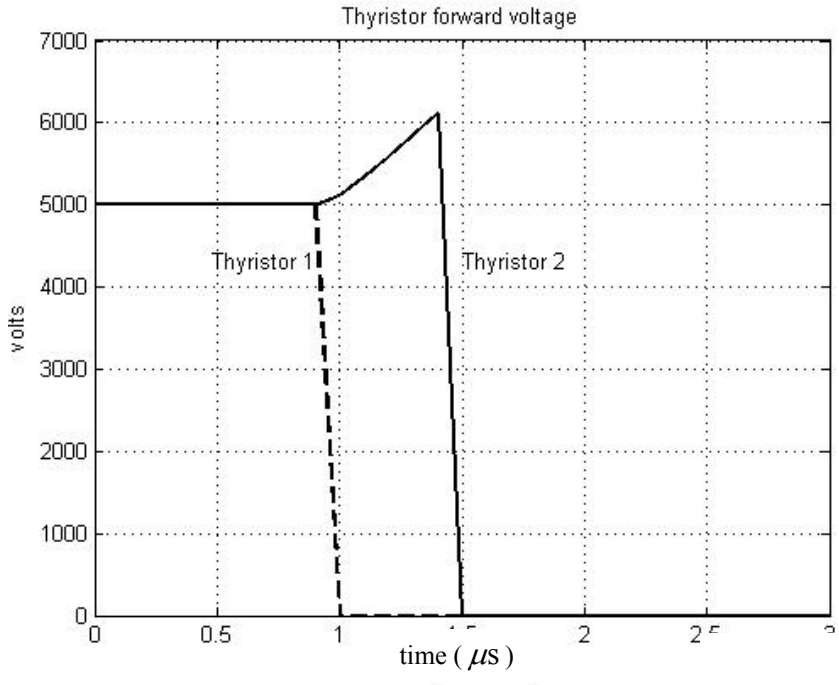

Figure 11. Simulated thyristor voltage sharing when the turn-on differs by 0.5 μs

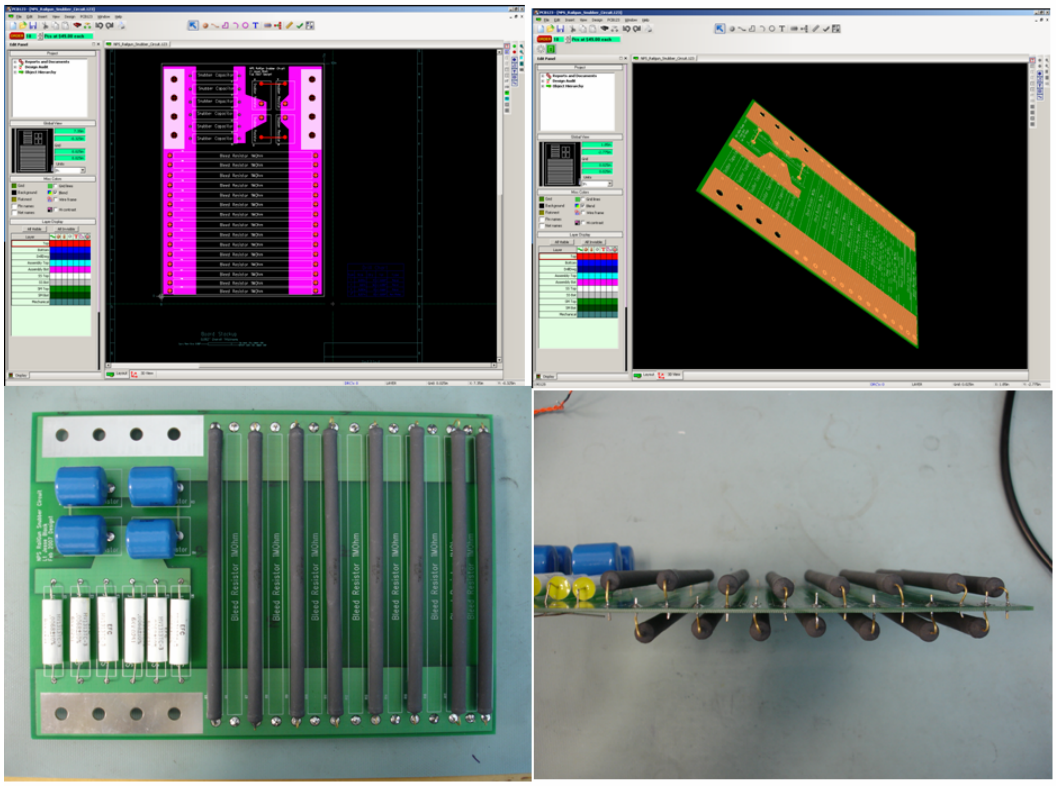

Figure 12. Snubber circuit pictures from top left moving clockwise. PCB123 board layout, PCB123 3-D View, Side view, Top View.

4. Summary

The model that was shown in Figure 10 for the subsystem in the power supply design was used for determining the values of the components of the snubber circuit. Figure 11 shows that thyristor 1 and 2 share voltage up until the time when the first thyristor is triggered. With out triggering the second thyristor, voltage begins to build up. Figure 11 shows that with the modeled components the second thyristor must be triggered within 0.5 µs to stay well within the 6500 V_{DSM} limit.

C. GATE CONTROL CIRCUIT

1. Introduction

The objective of the gate control circuit was to simultaneously turn on both thyristors by taking a single input light signal and converting it into two equivalent

current pulses. Sections C-2 through C-4 go into detail on how this was accomplished. One of the main objectives of this thesis was to ensure that the thyristors were kept from false triggering, Section C-5 covers this in detail along with describing the circuit protection.

2. Signal Conditioning for One Gate Control Circuit

The recommended current waveform for triggering the thyristors was provided in the data sheet and is shown in Figure 13. This waveform was the driving factor in the gate control circuit design. A thyristor is a current-controlled bipolar semiconductor. In order to make sure the thyristor turns on when directed the device needs a current pulse (I_{GM}) between 2 and 5 A. As per the data sheet, see Appendix A, this current is not to exceed 10 A (I_{FGM}). The time frame in which to reach the 90 percent of the I_{GM} is less than or equal to 1 µs. The duration (t_{p1}) of this first pulse needs from 5 to 20 µs. The second pulse (t_{p2}) is used to ensure that the thyristor remains on for the entire event. The intent of this design was to apply the first current pulse at 5 A for 20 µs and then apply the second pulse for 0.5 A for 10 ms. To create the single current waveform two separate pulses were magnetically coupled together into a single output, I_{g3}. I_{g3} is shown in Figure 13. The first pulse will be set to 20 µs and the second pulse will be set to 10 ms. R_{g1} will set I_{g1} to 5 A and R_{g2} will set I_{g2} to 0.5 A.

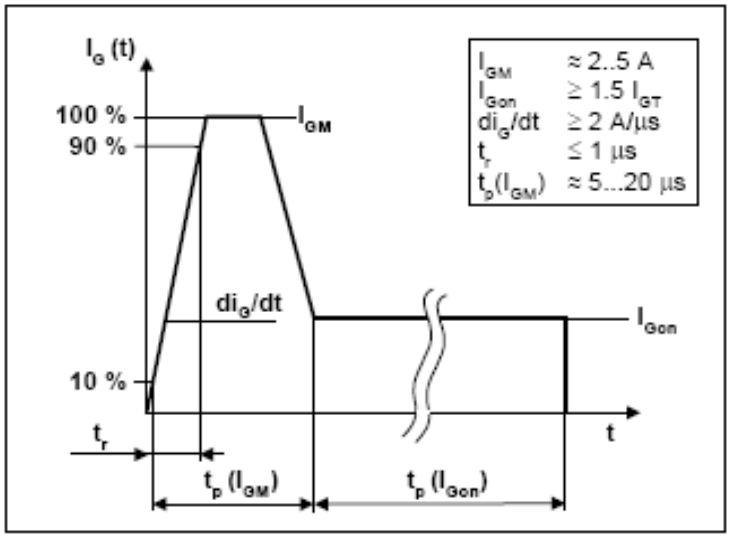

Figure 13. Recommended gate current waveform [from Ref 6].

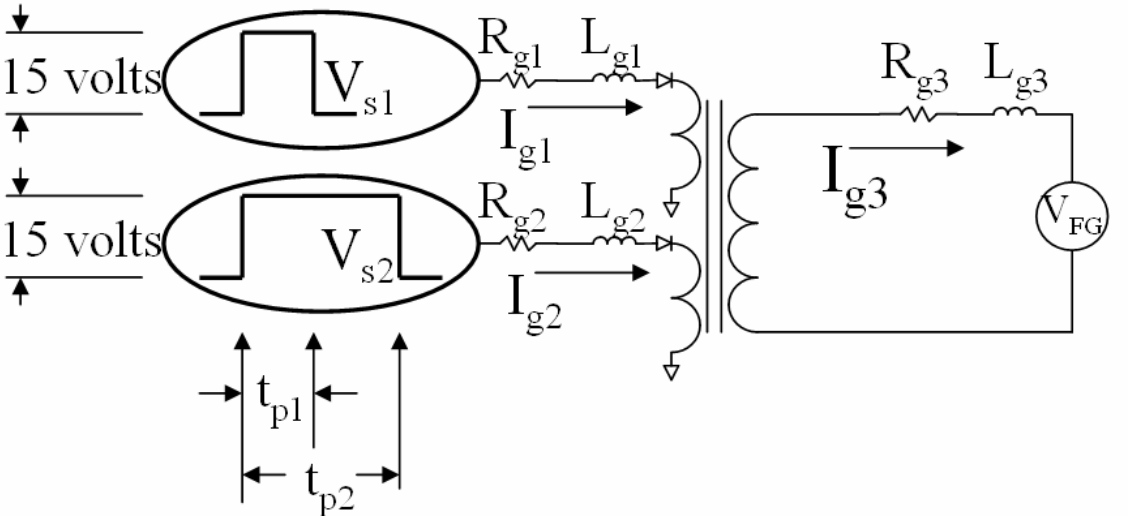

Figure 14. Gate driver equivalent circuit.

Figure 16 is the circuit diagram of the gate driver circuit and Figure 17 is a picture of the same circuit. Each of these figures have been broken into 8 sections to better aid in the following circuit description.

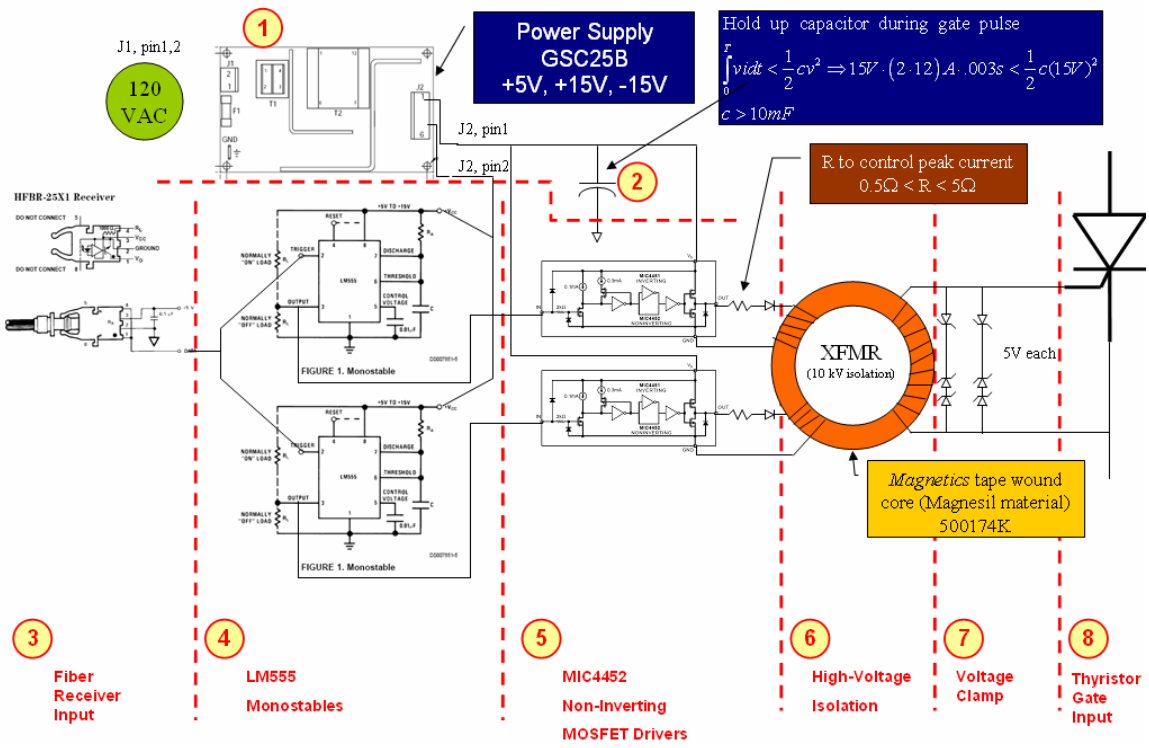

Figure 15. Gate Control Circuit.

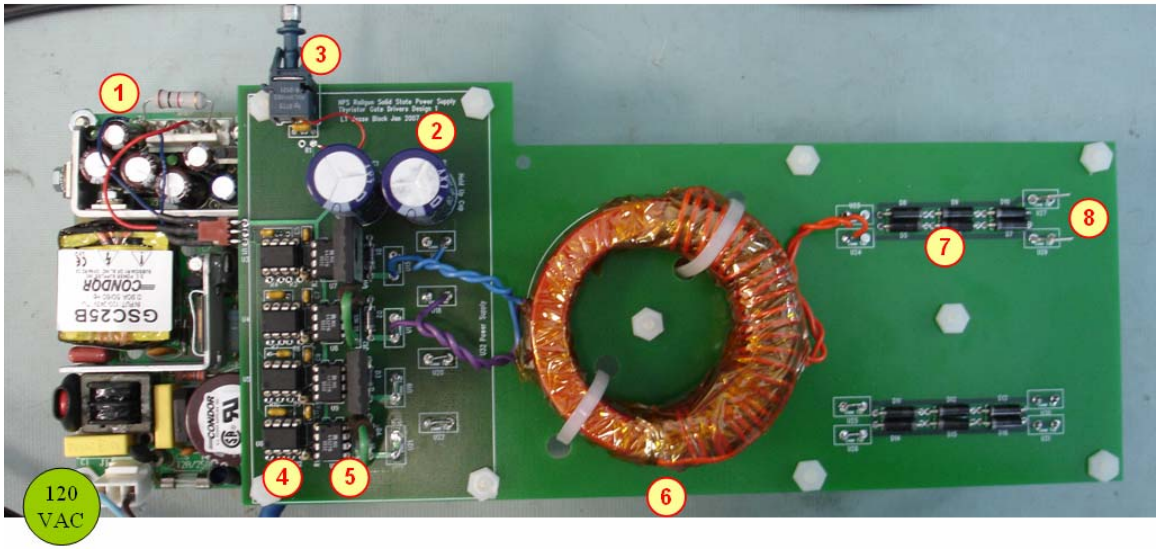

Figure 16. Top down view of Gate Control Circuit.

Section 1 is an off-the-shelf GSC25 Low-Voltage Power Supply (LVPS) purchased from Global Performance Switchers. It takes 120 VAC and converts it into +5/+15 VDC. Maximum current on the output for the +5 and + 15 V is 2.5 and 1.5 A respectively. The LVPS is fully protected against short circuit and output overload.

Short circuit is cycling type power limit [7]. Two modifications were made to incorporate this LVPS. First, a bleed resistor of 1.0 kΩ added as a continuous load to the +15 V terminal and ground terminal to ensure that the LVPS stayed in a continuous regulation state. The bleed resistor also gives a path for the holdup capacitors to discharge when the power supply is turned off. The second modification to the LVPS is described in the next paragraph.

Section 2 of the gate driver circuit is comprised of two 16 V 5600 μF holdup capacitors. As mentioned in the previous paragraph, the output current limit on the +15 V power supply is 1.5 A. Without these capacitors the LVPS would be driven into an overload condition and the desired current waveforms would not be produced. The following energy balance calculation was made to determine the capacitance needed to ensure the two that the current pulses were maintained.

$$CAP = \int_0^T Vidt < \frac{1}{2}cV^2 \Rightarrow 15 \cdot (2 \cdot 12) \cdot 0.003(VAs) < \frac{1}{2}c(15V)^2$$
$$\Rightarrow c > 10mF$$

To obtain the minimum capacitance needed the capacitors have to be able to drive the largest desired current pulse. This pulse is defined as pair of 15 V, 12 A, 3 ms pulses and therefore, the minimum capacitance needed would be 10 mF.

Section 3 highlights the fiber receiver. The device chosen here is the HFBR-2521. The output of this device is held high until the light pulse is received. Once this happens the output goes low and triggers the next devices. A critical point to mention is that the trigger pulse duration has to be less than t_{p1} as defined in section II.C.2. Power comes from the +5V of the LVPS.

The next section is section 4 and is comprised of two LM555 Monostable timer circuits. The LM555s are each accompanied by the RC network needed to set the output timing and one 0.01 μF capacitor for filtering. Once the input is a signal goes from high to low, the output is inverted and goes from low to high based off the values of the RC network. Figure 17 from LM555 data sheet and Table 1 show the resistor and capacitor

values need to set the timing pulse t_{p1} and t_{p2}. The data sheet refers to the timing pulse as the time delay t_d. The output of this stage is from low to high. Power for the LM555's comes from the +5 V LVPS.

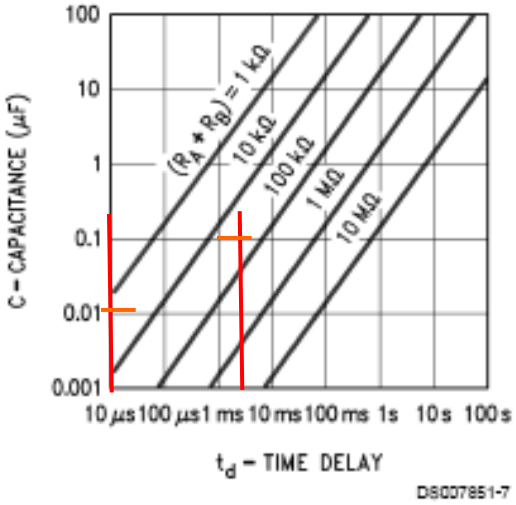

Figure 17. RA Values to set td based off specific C values. [from Ref (8)]

	t_{p1}	t_{p2}
R_A	1.49 kΩ	68.0 kΩ
C	0.01 μF	0.1 μF
t_d	10 μs	8 ms

Table 1. LM555 resistor and capacitor component values to set the timing for the current pulse I_{G1} and I_{G2}.

Now that the timing of the two pulses is set, the peak current of each pulse is established via a MIC4452 non-inverting MOSFET driver and resister combination. This is shown in section 5 of Figure 16 and 17. From Figure 14 the voltage drop on the resistor R_g will set the current I_g. Table 2 shows the values of R_{g1} and R_{g2} needed to obtain I_{g1} and I_{g2}. For protection a schottky diode was put in before the transformer to prevent reverse current back onto the drivers. Power for the drivers comes from the +15*V* LVPS.

	I_{G1}	I_{G2}
R	2.2 Ω	22 Ω
Peak Current	5 A	0.0A

Table 2. Resistance values to set I_{G1} and I_{G2}.

Section 6 is the high voltage isolation section of the gate driver. Magnetic coupling of the control circuit was critical due to the high blocking voltage on the thyristor which is coupled through the gate. The transformers are 500174K Magnetics tape wound core made of magnesil material. The major design consideration here was to minimize leakage flux while ensuring the magnetic core did not saturate. After wrapping the primary windings on the core two layers of Kapton tape were used to isolate the primary windings from the secondary windings. The same was done again after wrapping the secondary windings onto the core. Details regarding the High Voltage (HV) isolation tape can be found in Appendix (C). The second function of the core was to combine the two current pulses I_{g1} and I_{g2} into a single output pulse I_{g3}. There are 25 windings on the core with a turns ratio of one.

Section 7 is the voltage clamp and it was designed to protect the gate to cathode from over-voltage. The clamp is made up of the two zener diode stacks placed in parallel with the output of the transformer and the gate/cathode of the thyristor. Each stack has a $10V$ breakdown voltage in the forward direction and $5V$ breakdown voltage in the reverse direction. Finally, section 8 is the output of the gate driver circuit and is connected to the gate and cathode of the thyristor.

3. Signal Sequencing for Both Gate Control Circuits

A second pulse, identical to the one described in the eight steps above, had to be produced within in $0.5\ \mu s$ as mentioned in Chapter II. As indicated in Figure 10, the model shows that the time difference between each thyristor turning on has to be less than $0.5\mu s$. All the sections that were described in the part II.C.2 were duplicated on the same board. The input light pulse also triggers the second set of LM555s. To save space

on the Printed Circuit Board (PCB) the second HV transformer was placed on the underside. See Figure 18. Care was taken during component layout to ensure all signal paths were of equivalent size and length.

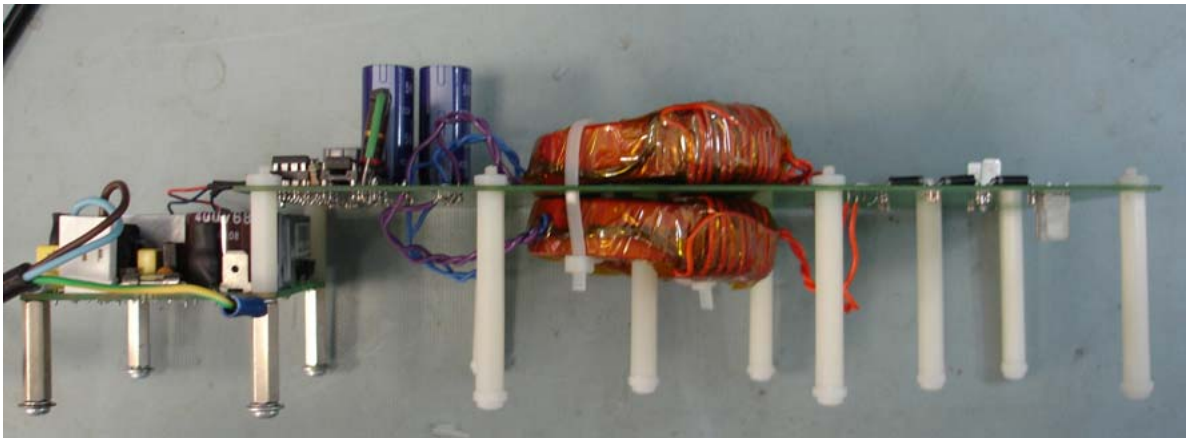

Figure 18. Side view of Gate Control Circuit

4. Model Simulation Using Matlab to Design the Transformers

Simulink was used to model the transformers. The purpose behind modeling the transformers was to determine if the transformers were going to saturate and thereby not let the current pulse be transferred to the secondary coil. The manufactures data was put into the model along with the component values of resistors that set I_{G1} and I_{G2} listed in Table 2. See Appendix (B) for the MATLAB code used to set these values. Figure 19 shows the model. Three state conditions exist for the model. The first is when both I_{G1} and I_{G2} turn on. The second is when I_{G1} is turned off and I_{G2} is still applied, and the third is when both I_{G1} and I_{G2} are both off. Figure 20 shows the details of each of subsystems and Figure 21 shows the output current. The blue trace is I_{G1}, the green is I_{G2} and the red trace is I_{G3}.

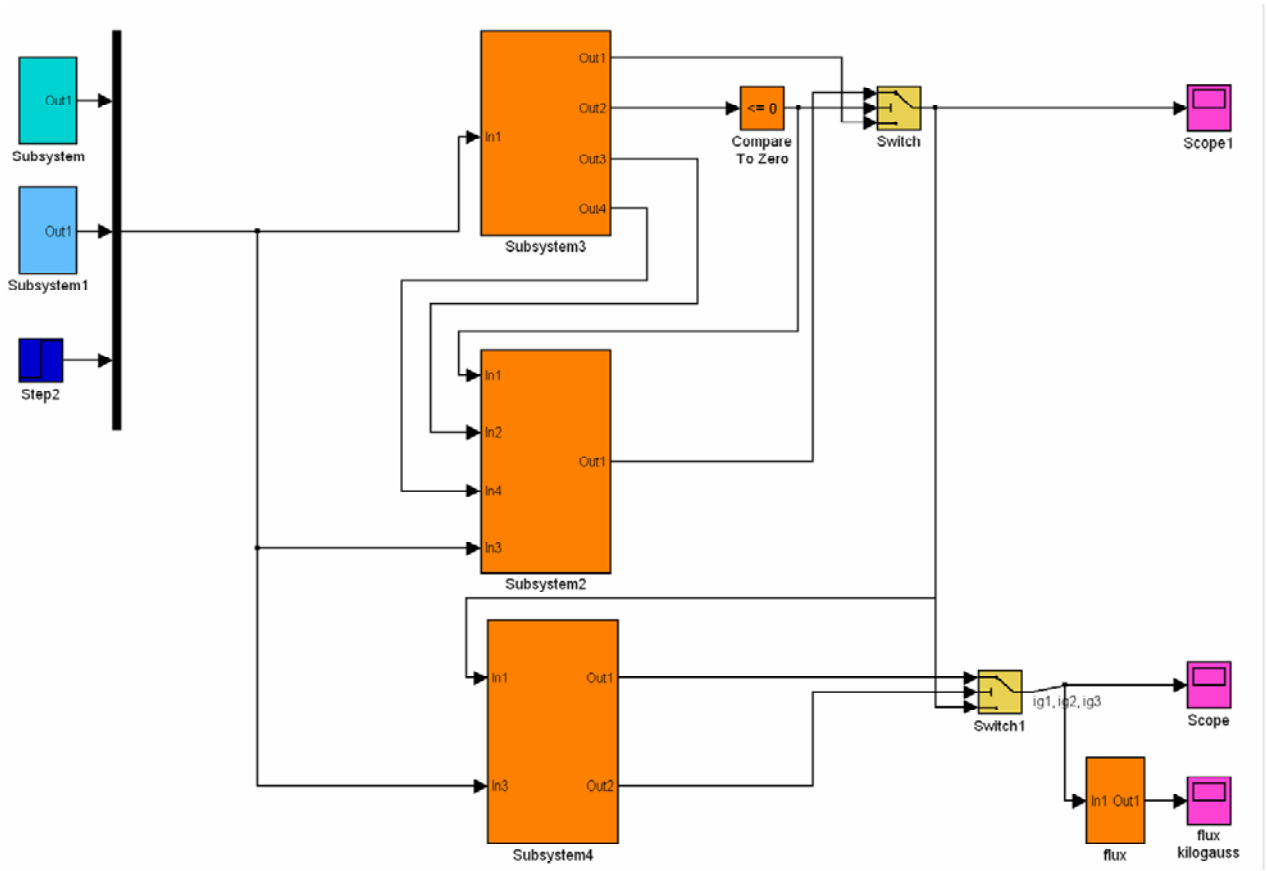

Figure 19. Simulink Transformer Model to Determine Values of Rg1 and Rg2.

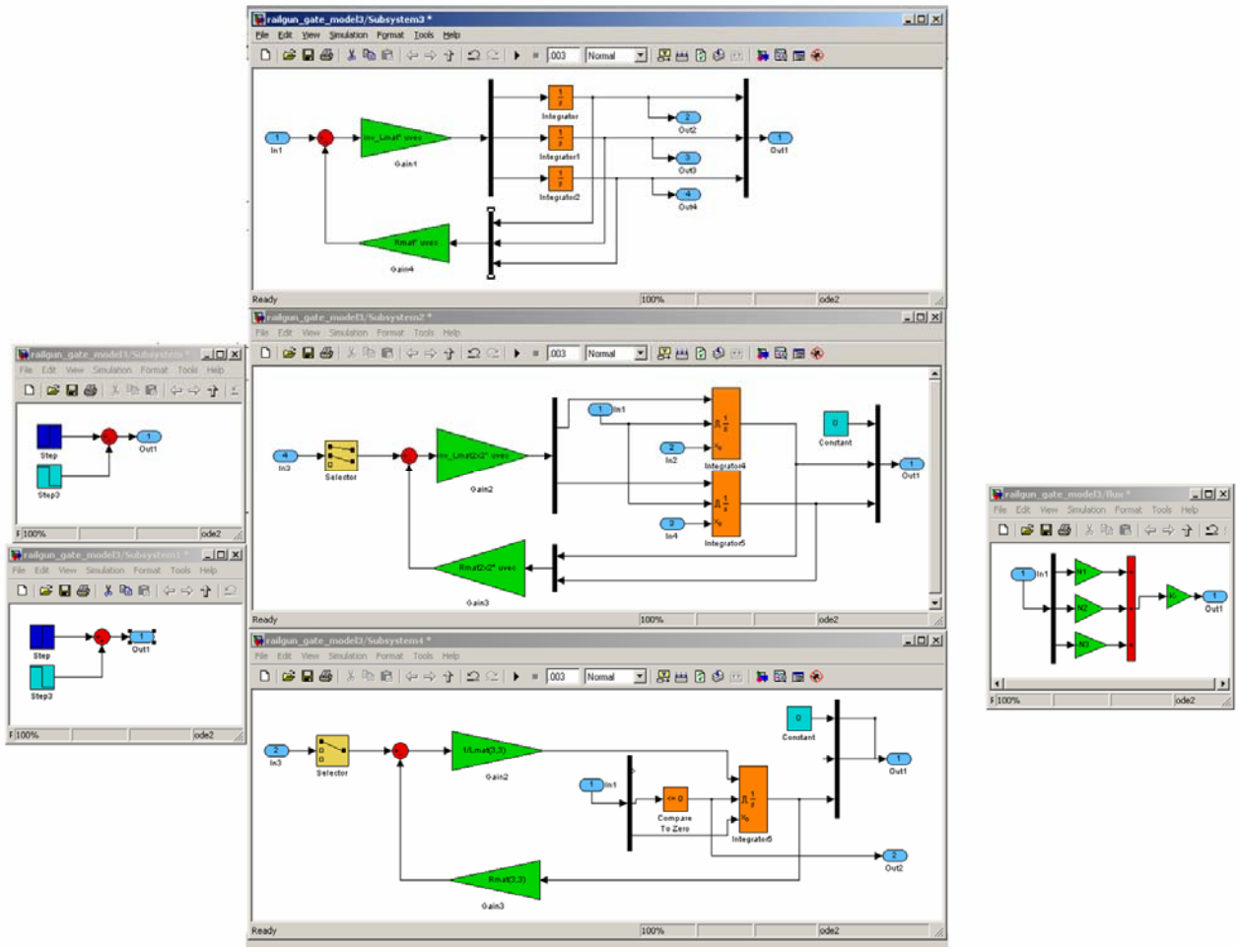

Figure 20. Details of subsystem in Simulink Model.

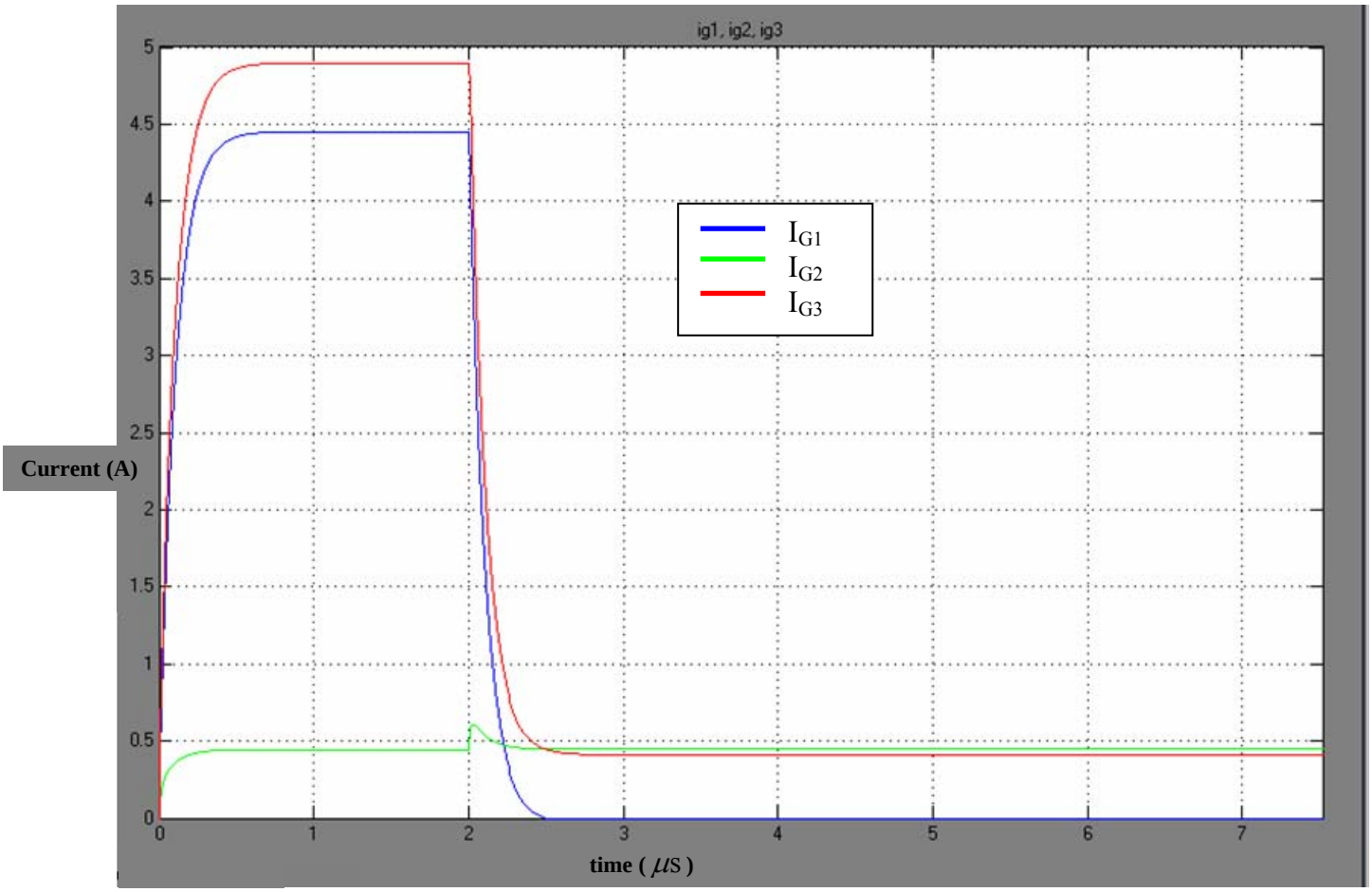

Figure 21. Simulated current pulses from the Simulink Transformer Model.

5. False Triggering Suppression and Circuit Protection

False triggering is a major concern when using thyristors in a noisy environment. To use this design to its fullest extent it has to be able to work in proximity to spark gap power supplies. These supplies produce significant EMP. Electrical isolation and shielding was incorporated into the design to keep the thyristors from false triggering. Figure 22 from the ABB data sheets specifies a minimum value for the gate-trigger current (I_{GT}) to be greater than 400 mA and a gate-trigger voltage (V_{GT}) to be greater than 2.6 V when operating the device at 25 °C. As the temperature of the device increases ABB states that the thyristor can potentially trigger on a gate signal of only 0.3 V and/or 10 mA; however, operation at room temperature is planned for this power supply.

Triggering

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110 °C	0.3			V
Gate non-trigger current	I_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110°C	10			mA

Figure 22. Maximum rated values for triggering [from Ref 6].

Isolation is accomplished in these layers via two transformers. The first isolation from the 120 VAC from the wall outlet to the output of the LVPS will block any disturbances being fed back from the outlet. The second isolation, between the control circuits and the gate/cathode connections, will prevent high voltage from being fed back to the control circuit and thereby causing damage. Figure 25 shows the two isolation transformers outlined in blue.

Shielding was incorporated to suppress possible EMP and was accomplished via two methods. A copper ground plane was chosen for high frequency protection copper and for low frequency protection a mumetal box encases the entire circuit board. Figure 23 shows the process of calculating the attenuation loss in dB based off the thickness of the material used and the skin depth of each material. The thickness of the mumetal is 0.035 in and by taking the ratio of the thickness to the skin depths Figure 23 produces an attenuation of 15 dB at 60 Hz and 90 dB of attenuation at 1 kHz. The thickness of the copper is 0.0014 in. Following the same process yields attenuation of 15 dB at 10 MHz and 90 dB at 1 GHz. The yellow box in Figure 25 shows where the copper ground plane is located on the gate control PCB. The mumetal box is not shown.

Table 6-2 Skin Depths of Various Materials

Frequency	Copper (in.)	Aluminum (in.)	Steel (in.)	Mumetal (in.)
60 Hz	0.335	0.429	0.034	0.019
100 Hz	0.260	0.333	0.026	0.011
1 kHz	0.082	0.105	0.008	0.003
10 kHz	0.026	0.033	0.003	—
100 kHz	0.008	0.011	0.0008	—
1 MHz	0.003	0.003	0.0003	—
10 MHz	0.0008	0.001	0.0001	—
100 MHz	0.00026	0.0003	0.00008	—
1000 MHz	0.00008	0.0001	0.00004	—

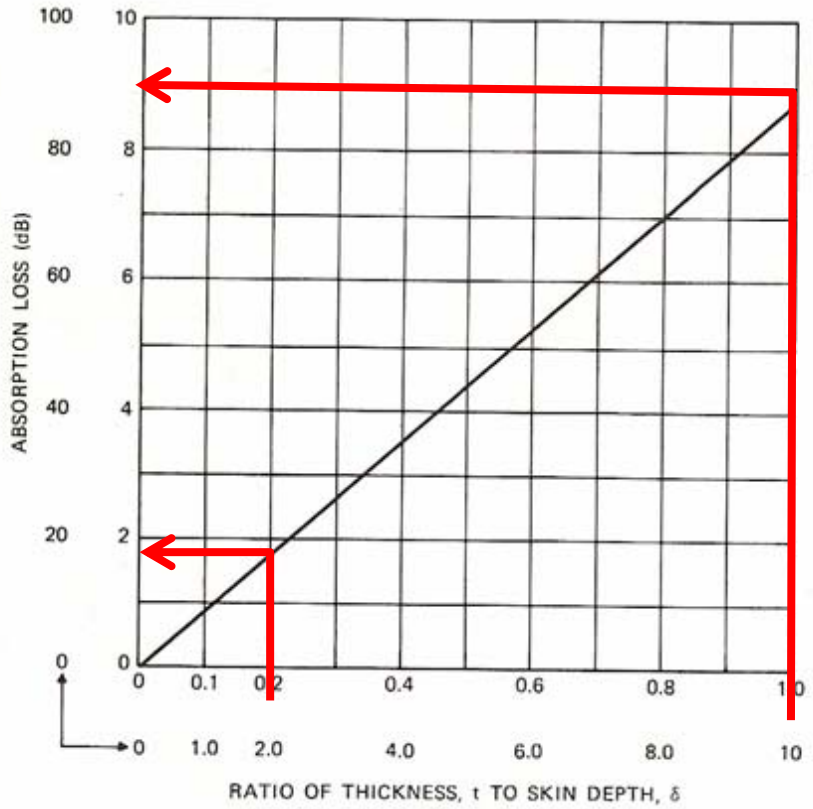

Figure 6-7. *Absorption loss is proportional to the thickness and inversely proportional to the skin depth of the medium. This plot can be used for electric fields, magnetic fields, or plane waves.*

Figure 23. Table and chart of computing attenuation for shielding [from Ref 9].

To minimize pickup all the control signals were kept to a minimum length and were placed in the inner layer of the PCB.

Minimum creepage and clearance was also a concern and had to be maintained. Figure 24 lists the minimum surface creepage distance to be 56 mm (2.2 in) and the minimum air strike distance to be 22 mm (0.86 in). The red arrows in Figure 25 show the major points of contention. Each of these lines will be a minimum of 1 in. As mentioned above, the transformers are wrapped in Kapton tape with each layer of tape rated to block 10 kV.

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				3.6	kg
Housing thickness	H	F_M = 135 kN, T_a = 25 °C	34.8		35.5	mm
Surface creepage distance	D_S		56			mm
Air strike distance	D_a		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

Figure 24. Minimum surface creepage distance and air strike distance.

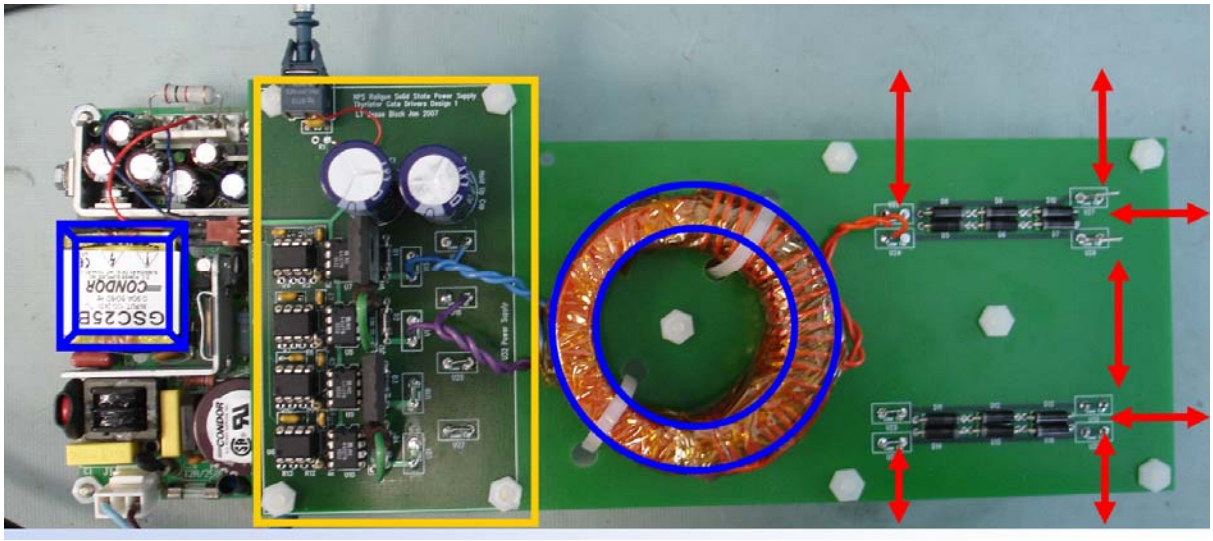

Figure 25. EMP Suppression and Creepage and Clearance.

6. Summary

Although this circuit may seem simplistic it was paramount that an identical current pulse be delivered to each thyristor at nearly the same time. It was critical that the circuit be designed to prevent a false triggering of the thyristors. These objectives were accomplished by using shielding for noise suppression. Isolation transformers were used to protect the LVPS and control circuit from the outlet and from the high voltage on the thyristors. Finally the physical layout of the components maintains the minimum creepage and clearance distances. PCB123 was used to for the design layout and is shown in Figure 26 and Figure 27.

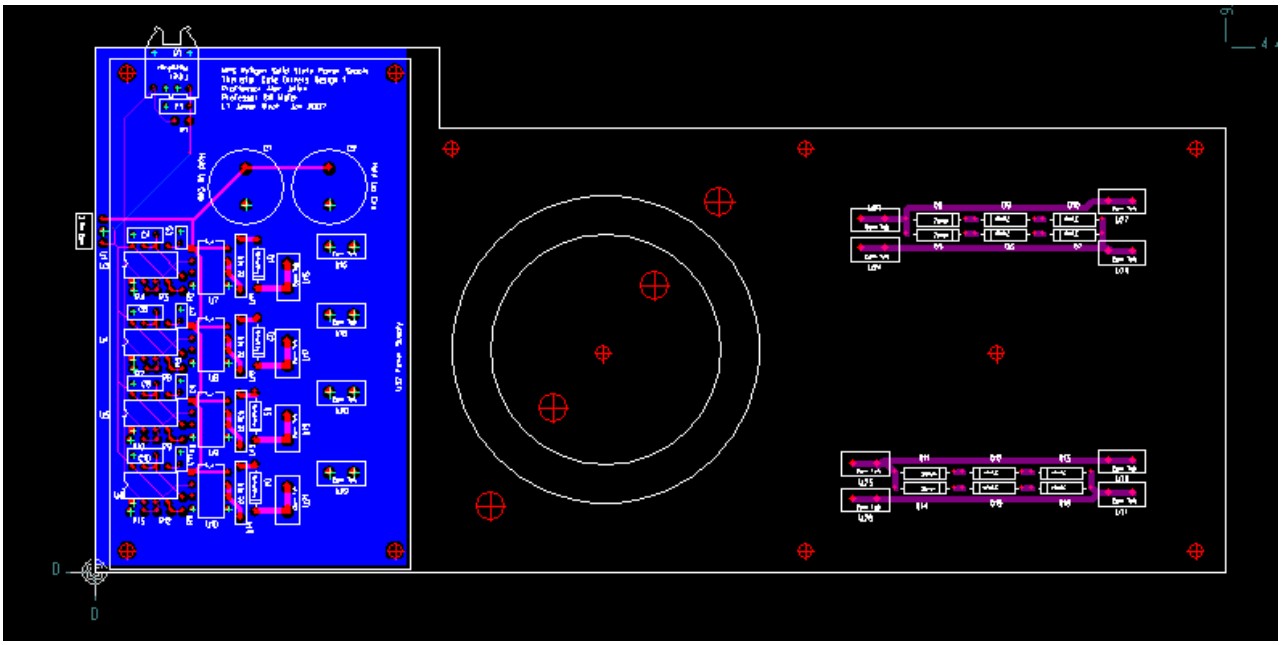

Figure 26. PCB 123 top view of the gate control circuit.

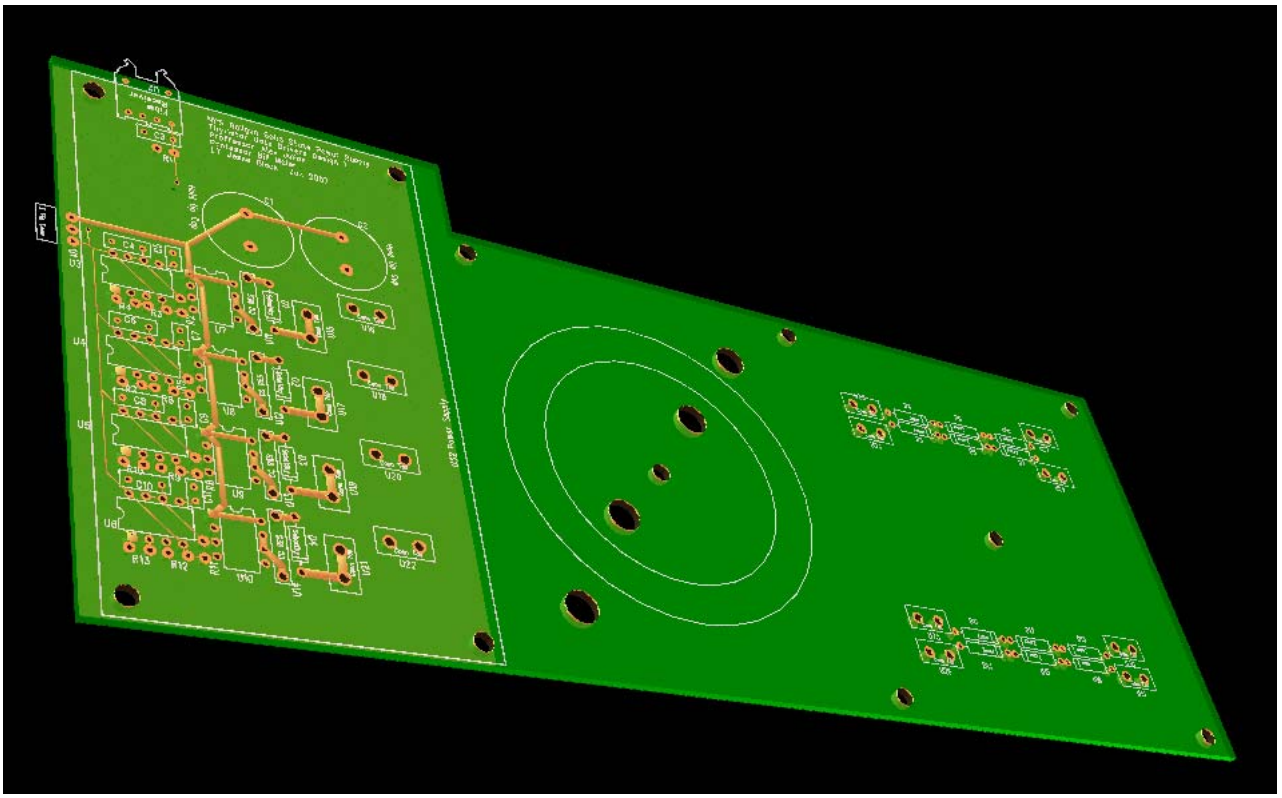

Figure 27. PCB123 3-D view of the gate control circuit.

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III. EXPERIMENTAL DATA ACQUISITION FOR GATE CONTROL CIRCUIT

A. INTRODUCTION

Three changes made from the initial design are described in section III. B. Data collection for the gate control circuit started by identifying the correct high voltage isolation transformer. Signal sequence testing was completed next, then the peak currents and timing were tested. Finally, the di/dt for the gate was measured to determine the circuit delay from the time between when the fiber pulse was sent and the start of both thyristors gate pulse signals.

B. CONSTRUCTION

Upon initial testing a problem with the power supply was noted. When measuring the +5 V or +15 V supply the reading would cycle up and then back down to zero. It was determined that the supply had to be under continuous load to regulate. A 1 kΩ resistor was added to the +15 V terminal and ground.

The board that was tested was the second of two built. On the first board a faulty LM555 had to be replaced. During the de-soldering the board was permanently damaged and caused the +5 V supply to be grounded. For the second board, chip sockets were used. These sockets were not used initially in trying to keep the signal traces small; however, final testing showed they did not adversely affect the circuit.

Initially a HRBF-2821 was chosen as the fiber receiver based on its performance as specified by the manufacture. Testing revealed it was not the same type of receiver as all the other HFBR-2X21; therefore, a receiver was used instead. A second socket with wire wraps and jumpers was used on top of the board socket to handle the changes in the in HFBR-2121 receiver's pinout.

C. DATA COLLECTION

1. High Voltage Isolation Transformer

To determine the most efficient coil, 4 different wire wrapped coils were made. Figure 28 shows the results of this testing. The blue trace is that of the fiber optic signal set to give a low voltage for $10\ \mu s$. I_{G1} is the blue wire and I_{G2} is the magenta wire. Each of the blue and magenta wires shown in the figure are the primaries. The secondary coil, I_{G3}, is the orange wire.

Core 1 has a turns ratio of N=1:1 with the core completely covered in the primary windings each having 43 turns. The secondary coil is tightly wrapped on the right half of the core. As the plot shows, this did not give the desired coupling with a low di/dt rise time.

For core 2 the primary windings were pulled back to match the area of the secondary. Now the turns ratio was N=1:2. Although this configuration had the desired coupling with a high di/dt, the current was now reduced by half.

Cores 3 and 4 are similar with a turns ratio of N=1:1 and the secondary loosely wrapped. The difference is core 3 is completely wound with 43 turns and core 4 is only wrapped half with 25 turns. Core 4 was chosen because of its slightly better performance.

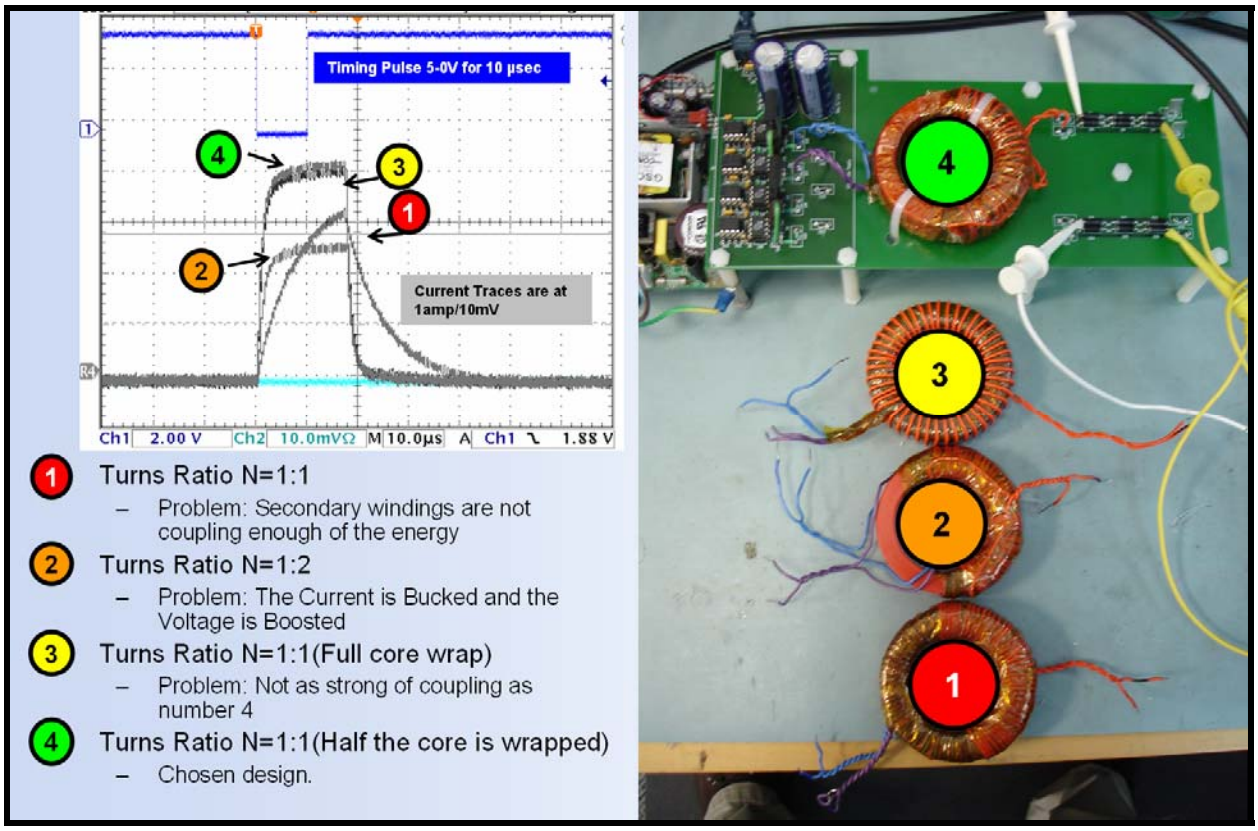
Timing Pulse 5-0V for 10 µsec
Current Traces are at 1amp/10mV
Ch1 2.00 V Ch2 10.0mVΩ M 10.0µs A Ch1 1.88 V
1 Turns Ratio N=1:1
– Problem: Secondary windings are not coupling enough of the energy
2 Turns Ratio N=1:2
– Problem: The Current is Bucked and the Voltage is Boosted
3 Turns Ratio N=1:1(Full core wrap)
– Problem: Not as strong of coupling as number 4
4 Turns Ratio N=1:1(Half the core is wrapped)
– Chosen design.
4
3
2
1

Figure 28. Results from transformer testing.

2. Sequence Testing

To test the circuit board two Integrated Bipolar Junction Transformers IGBTs were used for their PN junctions. This was to simulate the gate to cathode connections on the thyristors. A Pearson Transformer was used on each gate signal to measure the current. Figure 29 shows the test set up.

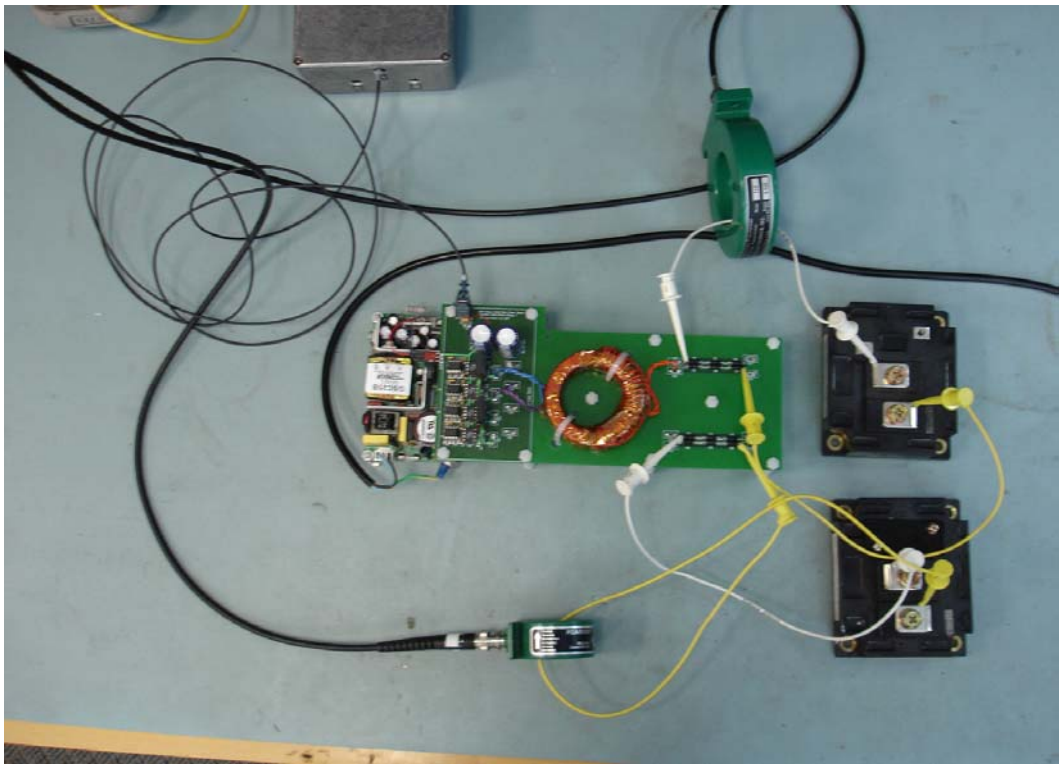

Figure 29. Gate control circuit test set up.

Figure 30 shows that both rise to 5 A in 20 μs and are held on at 0.5 A for at least. 50 μs This closely matches the desired from ABB as shown in Figure 31. Figure 32 shows that the delay from the time the fiber receiver sends the low pulse to the time I_{G3} starts to be 300 ns. Both I_{G3}s for each thyristor rise at the same time and reach the 90 percent of I_{GM} (defined as t_r in Figure 31) in1 μs .

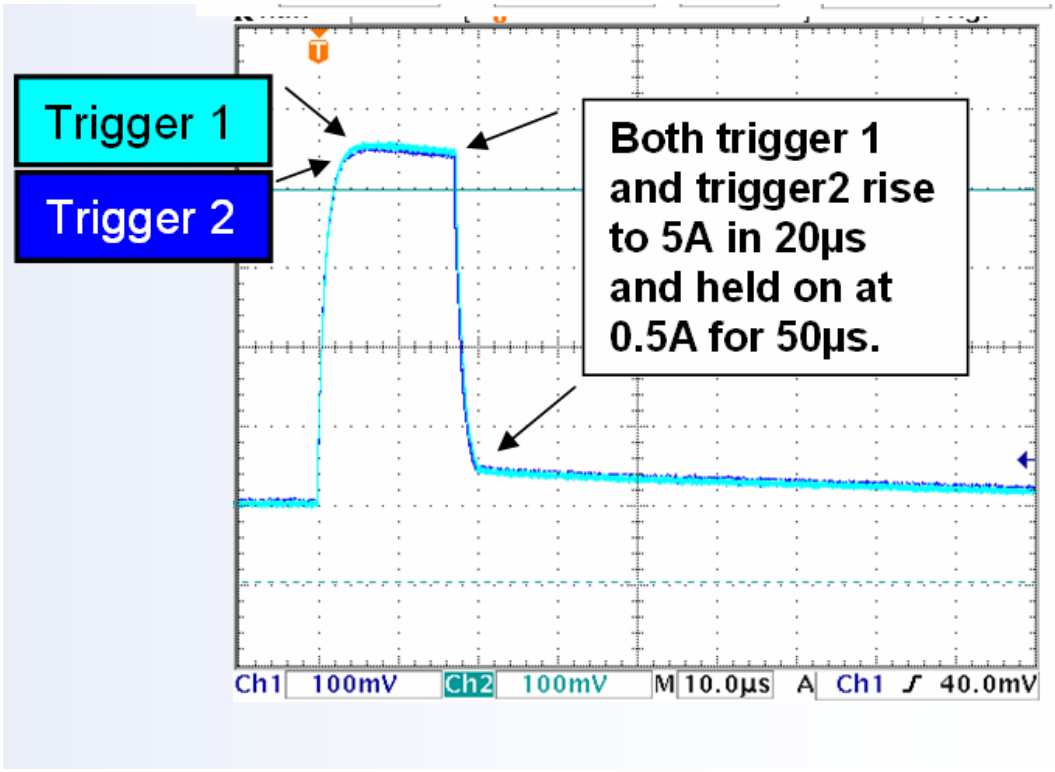
Trigger 1
Trigger 2
Both trigger 1 and trigger2 rise to 5A in 20µs and held on at 0.5A for 50µs.
Ch1 100mV
Ch2 100mV
M 10.0µs
A Ch1 ∫ 40.0mV

Figure 30. Output waveforms from the gate control circuit.

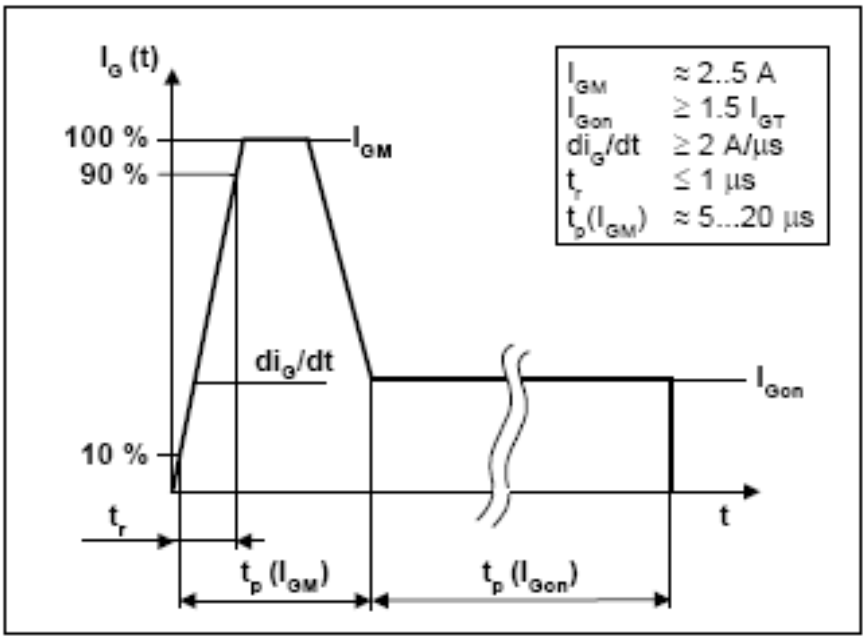

Figure 31. Recommended gate current waveform [from Ref 6].

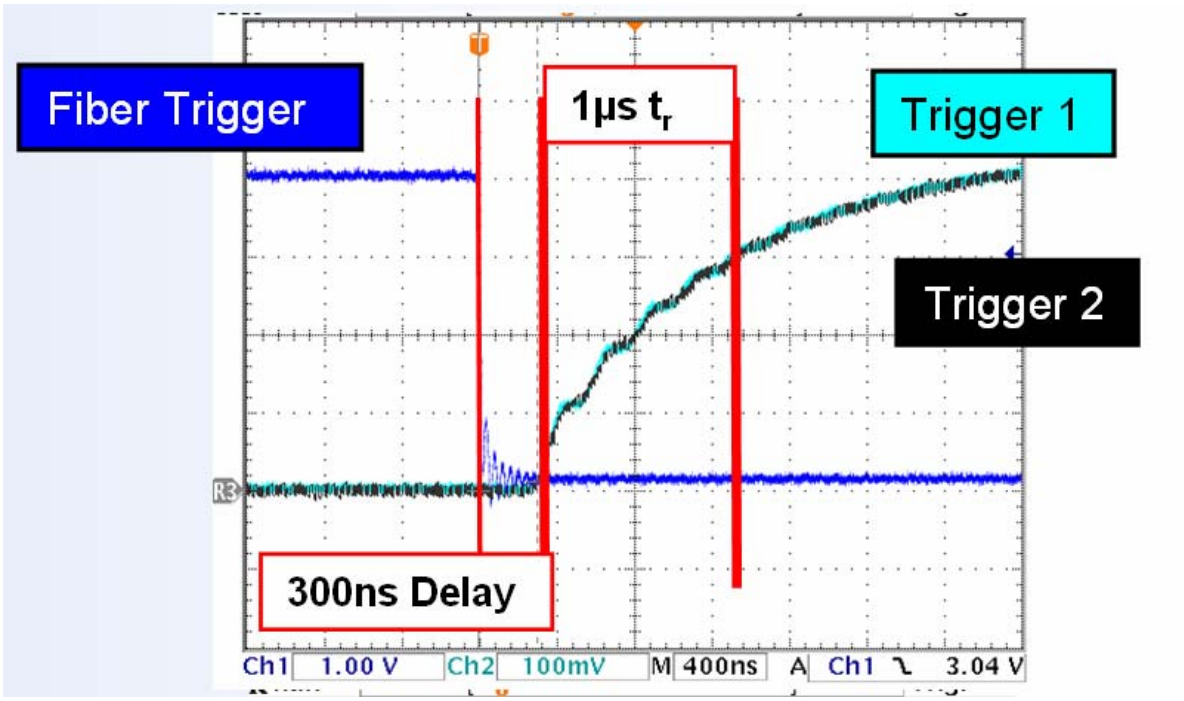

Figure 32. Gate control circuit time delay and rise time.

IV. CONCLUSIONS AND RECOMMENDATIONS

A. INTRODUCTION

The final chapter will start by covering a brief discussion on validation of the models and then it will move into discussing how the research question was answered. Because the fabrication of the entire supply was not completed the majority of the future work will reside in testing and optimizing these models. This chapter ends with conclusions.

B. VALIDATIONS OF MODELS

The gate control circuit model proved to be helpful in ensuring the magnetic cores were not going to saturate. Now the model can be used to see how changing components, such as the resistors, will affect the output current pulse. The models for both the snubber circuit and the railgun will be validated in future testing.

C. RESEARCH QUESTION ANSWERED

The intent of this thesis was to provide the Naval Postgraduate School Railgun Lab with a solid state power supply design. The supply was designed and now the supply is well on its way to final construction and testing. The snubber circuit was built and waits testing. The gate control circuit was built and bench tested. The results from the testing were better than expected with the delay between the two triggers so small it is said to be simultaneous.

D. FUTURE WORK

The next round of testing should include testing the gate control circuit next to the spark-gap power supplies when they are fired. This test will ensure that the false triggering mitigation designs work to an acceptable level. Next, the rest of this supply needs to be put together in a housing. Figure 33 shows the initial arrangement of parts in the proposed power supply. The thyristors (red and blue disks) and crowbar diodes (yellow and green disks) are clamped directly above the capacitor (blue upright

rectangular box) via a single clamp. The light green cylinder is the inductor. Figure 33 also shows the proposed placement of the snubber circuit boards. Figure 34 shows the spark-gap power supplies. Each of the two power supplies shown are placed in the same size housing as the proposed design in Figure 33. By reducing the volume of the switching components the inductor is now be placed inside the power supply hosing. Once the new supply is built testing and optimization for the entire system can then begin.

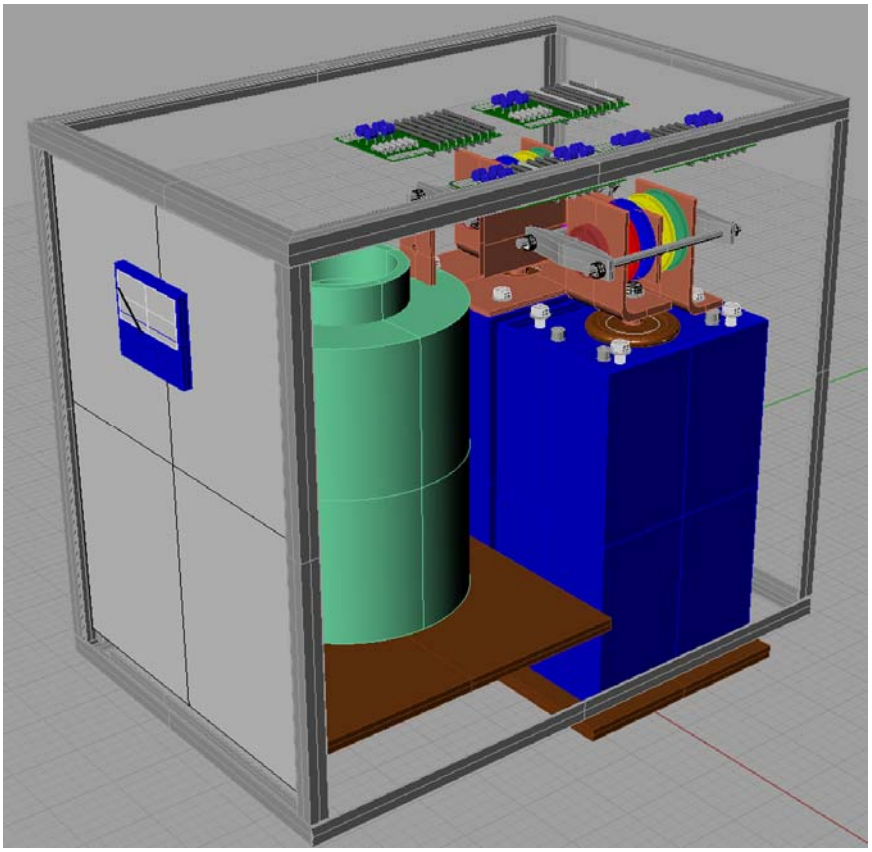

Figure 33. CAD drawings of the new power supply.

Figure 34. Picture of the spark-gap power supplies.

Future projects include modeling and observing how theses power supplies can be paralleled together to form a pulse forming network. Integrating the output inductor into the bus network would reduce the resistance of the power supply and has the potential for increasing the efficiency of the railgun.

E. CONCLUSIONS.

Although the final power supply was not completed and tested, much progress was made in converting over from the expensive, noisy, non-efficient, and larger power supplies to a new design that will be cheaper, less-noisy, more efficient, and smaller. Using commercial products to do military applications is not straight forward. Because this application is so different than the planed intent a new data sheet will be written from future testing. In turn, this will allow the purchase of even smaller devices or allow more capacitors to be controlled by a single thyristor.

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APPENDIX A

V_{DRM}	= 5600	V
V_{DSM}	= 6500	V
$I_{T(AV)M}$	= 3460	A
$I_{T(RMS)}$	= 5440	A
I_{TSM}	= 71.4×10^3	A
$V_{(T0)}$	= 1.24	V
r_T	= 0.162	mΩ

Phase Control Thyristor

5STP 42U6500

Doc. No. 5SYA1043-02 Oct. 04

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values [1]

Symbol	Conditions	5STP 42U6500	5STP 42U6200	5STP 42U5800
V_{DSM}, V_{RSM}	f = 5 Hz, t_p = 10 ms	6500 V	6200 V	5800 V
V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms	5600 V	5300 V	4900 V
V_{RSM}	t_p = 5 ms, single pulse	7000 V	6700 V	6300 V
dV/dt_{crit}	Exp. to 3750 V, T_{vj} = 110°C	2000 V/µs		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DSM}	V_{DSM}, T_{vj} = 110°C			700	mA
Reverse leakage current	I_{RSM}	V_{RSM}, T_{vj} = 110°C			700	mA

Mechanical data

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				3.6	kg
Housing thickness	H	F_M = 135 kN, T_a = 25 °C	34.8		35.5	mm
Surface creepage distance	D_S		56			mm
Air strike distance	D_a		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

ABB Switzerland Ltd, Semiconductors reserves the right to change specifications without notice.

On-state

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AVM)}$	Half sine wave, T_c = 70°C			3460	A
RMS on-state current	$I_{T(RMS)}$				5440	A
Peak non-repetitive surge current	I_{TSM}	tp = 10 ms, T_{vj} = 110 °C, $V_D = V_R$ = 0 V			71.4×10^3	A
Limiting load integral	I^2t				25.48×10^6	A^2s
Peak non-repetitive surge current	I_{TSM}	tp = 8.3 ms, T_{vj} = 110 °C, $V_D = V_R$ = 0 V			76.14×10^3	A
Limiting load integral	I^2t				24.64×10^6	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 3000 A, T_{vj} = 110 °C			1.71	V
Threshold voltage	$V_{(TO)}$	I_T = 2000 A - 6000 A, T_{vj} = 110 °C			1.24	V
Slope resistance	r_T				0.162	mΩ
Holding current	I_H	T_{vj} = 25 °C			200	mA
		T_{vj} = 110 °C			100	mA
Latching current	I_L	T_{vj} = 25 °C			900	mA
		T_{vj} = 110 °C			700	mA

Switching

Maximum rated values [1]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	dI/dt_{crit}	T_{vj} = 110 °C, I_{TRM} = 3000 A,	Cont. f = 50 Hz			250	A/µs
Critical rate of rise of on-state current	dI/dt_{crit}	$V_D \leq$ 1680 V, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 1Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 110°C, I_{TRM} = 3000 A, V_R = 200 V, dI_T/dt = -1 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20V/µs		800			µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_r	T_{vj} = 110°C, I_{TRM} = 3000 A, V_R = 200 V, dI_T/dt = -1 A/µs	4200		5200	µAs
Gate turn-on delay time	t_{gd}	$V_D = 0.4 \cdot V_{RM}$, I_{FG} = 2 A, t_r = 0.5 µs, T_{vj} = 25 °C			3	µs

Triggering

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$			see Fig. 9		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110 °C	0.3			V
Gate non-trigger current	I_{GD}	V_D = 0.4 x V_{DRM}, T_{vjmax} = 110°C	10			mA

Thermal

Maximum rated values [1]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				110	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 120...160 kN			4	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 120...160 kN			8	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 120...160 kN			8	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 120...160 kN			0.8	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 120...160 kN			1.6	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_{th\,i}(1 - e^{-t/\tau_i})$$

i	1	2	3	4
$R_{th\,i}$(K/kW)	2.695	0.614	0.330	0.162
τ_i(s)	0.9692	0.1332	0.0177	0.0042

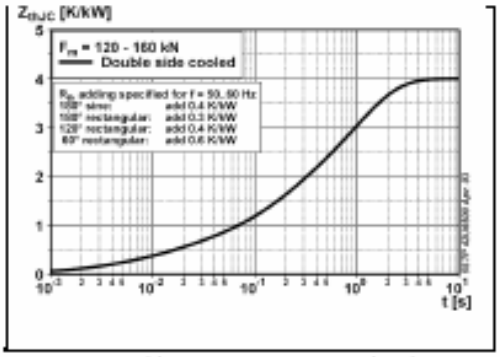

Fig. 1 Transient thermal impedance junction-to case.

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 800 – 100000 A

A_{25}	B_{25}	C_{25}	D_{25}
123.80×10^{-6}	91.68×10^{-6}	192.1×10^{-3}	-2.91×10^{-3}

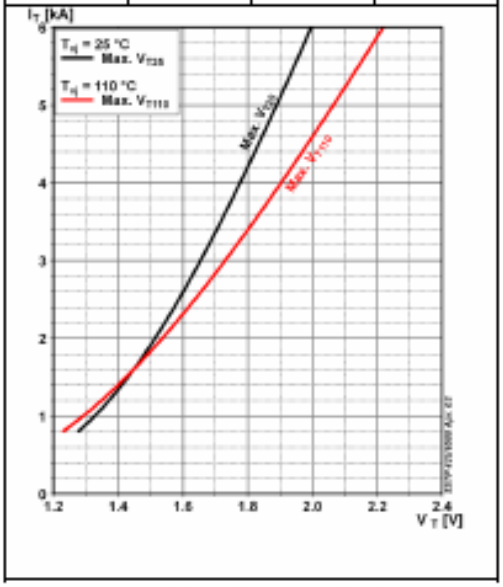

Fig. 2 Max. on-state voltage characteristics

Max. on-state characteristic model:

$$V_{T110} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 800 – 100000 A

A_{110}	B_{110}	C_{110}	D_{110}
136.10×10^{-6}	117.20×10^{-6}	165.60×10^{-3}	957.50×10^{-6}

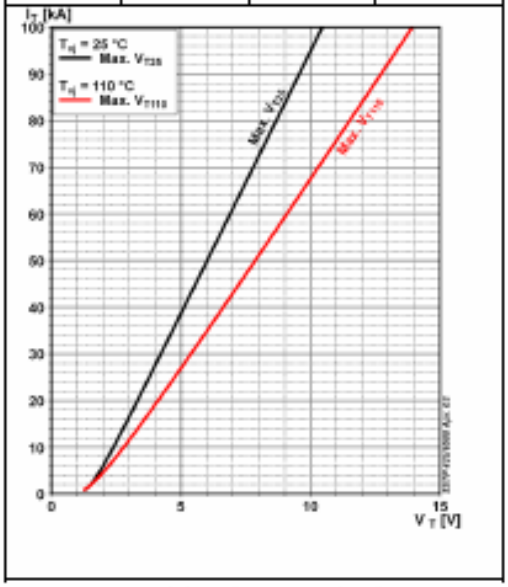

Fig. 3 Max. on-state voltage characteristics

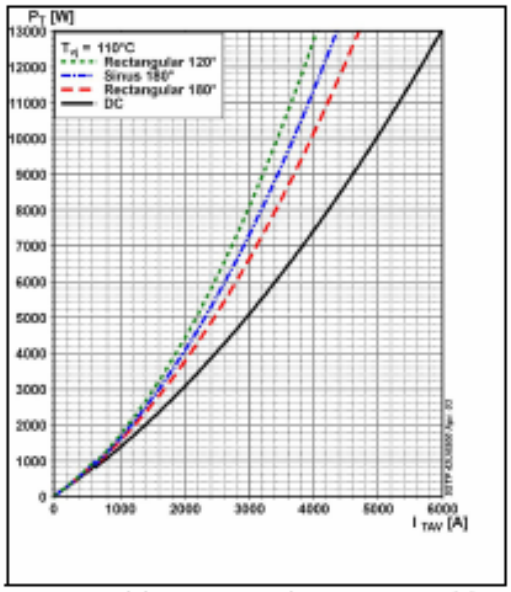

Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

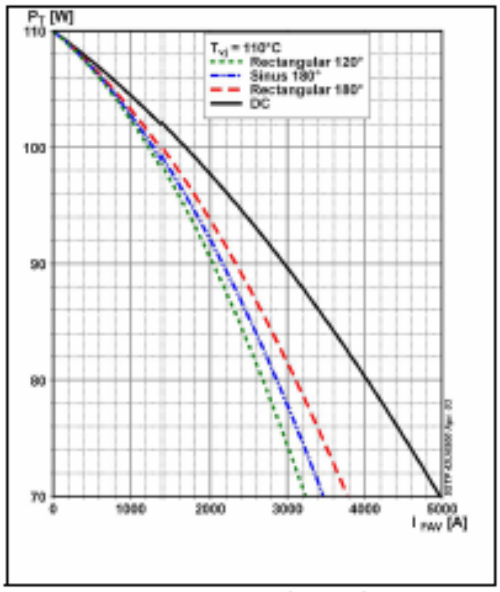

Fig. 5 Max. permissible case temperature vs. mean on-state current.

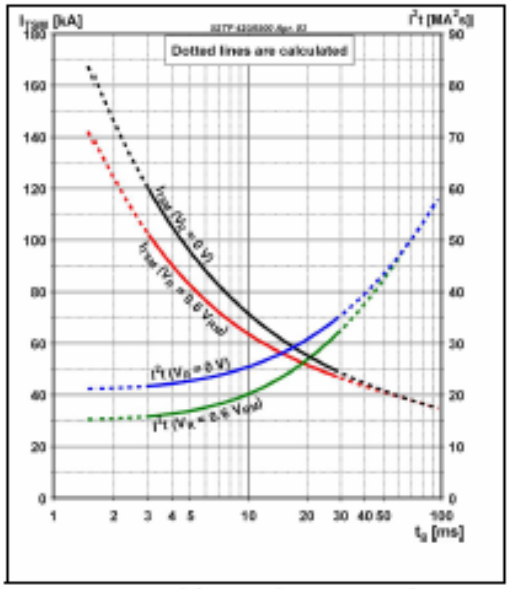

Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

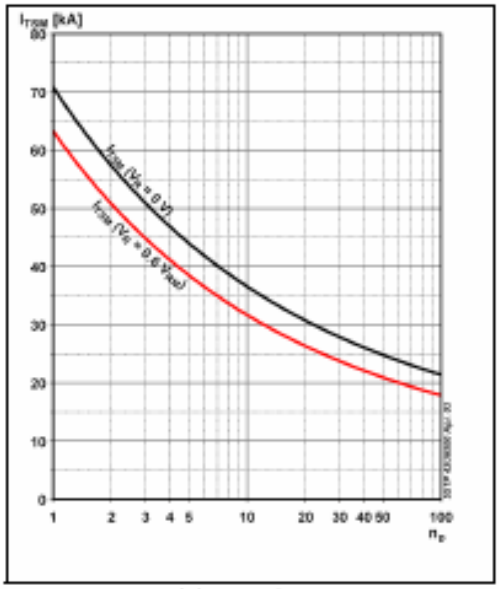

Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

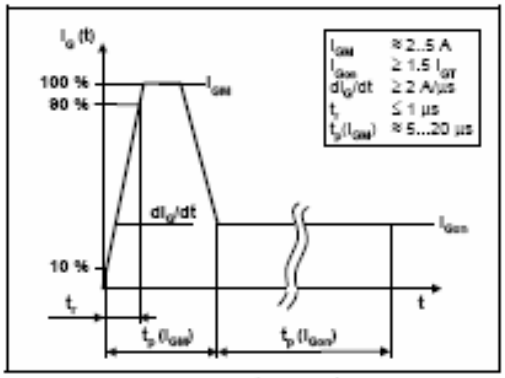

Fig. 8 Recommended gate current waveform.

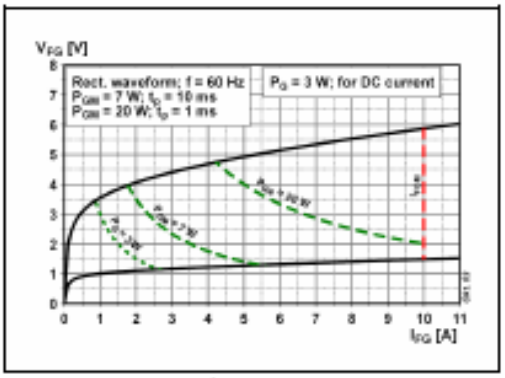

Fig. 9 Max. peak gate power loss.

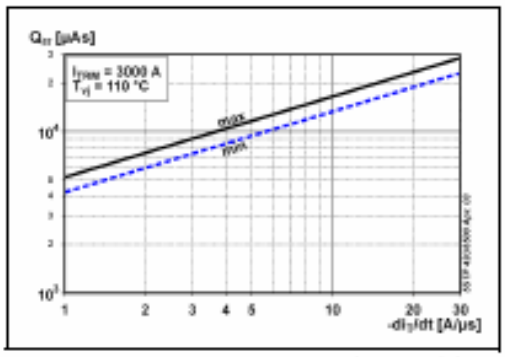

Fig. 10 Recovery charge vs. decay rate of on-state current.

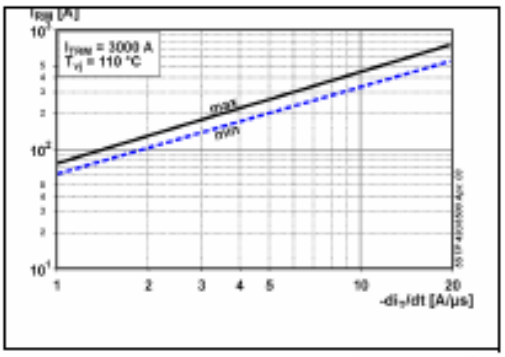

Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

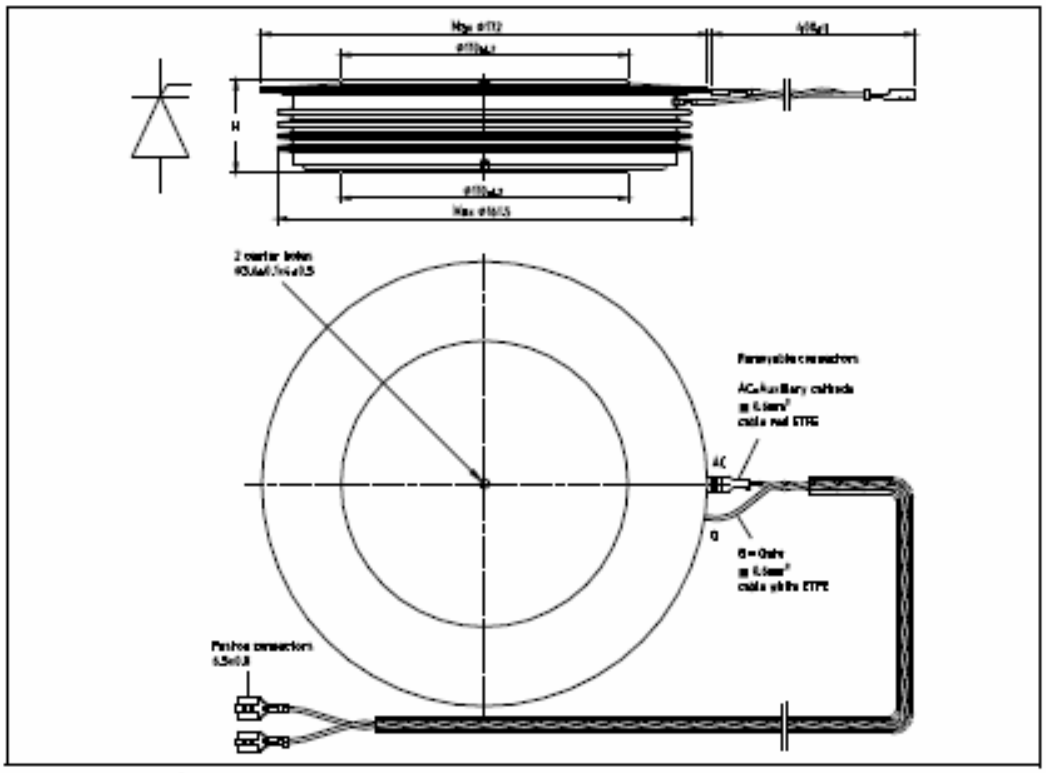

Fig. 12 Device Outline Drawing.

Related application notes:

Doc. Nr	Titel
5SYA2020	Design of RC-Snubber for Phase Control Applications
5SYA2034	Gate-drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors

Please refer to http://www.abb.com/semiconductors for actual versions.

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ABB Switzerland Ltd
Semiconductors
Fabrikstrasse 3
CH-5600 Lenzburg, Switzerland

Telephone +41 (0)58 586 1419
Fax +41 (0)58 586 1306
Email abbsem@ch.abb.com
Internet www.abb.com/semiconductors

Doc. No. 5SYA1043-02 Oct. 04

APPENDIX B

Matlab code for the transformer design:

```
%Transformer design equations
%Magnetics Magnesil tape wound toroid 50017, 4 mil material
%ID 2 inches, OD 2.5 inches, thickness 0.5 inches
%ID .0508 m , OD .0635 m   , thickness .0127 m
le=.1795;
Ae=.689/100^2   % meters^2
uo=4*pi*1e-3;
ur=40000;
le=.152;                              %meters
turns=25;    %Original Value
%turns=10;       %Changed Value
ipeak=24;
B=uo*ur*turns*ipeak/le/10^-4      %gausses
inductance=uo*ur*turns^2*Ae/le   %H
H2=0.4*pi*turns*ipeak/(le*100)  %oersteds

N1=turns;
N2=turns;
N3=turns;
Lleak=1e-6;   %Original
%Lleak=20e-6;    %Changed Value
L11=inductance;        %Convert to henries
L22=N2^2/N1^2*L11;L33=N3^2/N1^2*L11;
L12=N2/N1*L11;L21=L12;
L13=N3/N1*L11;L31=L13;
L23=N3/N2*L22;L32=L23;
%third coefficient is negative in each row because the winding polarity
is
%reversed.
Lmat=[L11+Lleak L12 -L13; L21 L22+Lleak*N2^2/N1^2 -L23; L31 L32 -L33-
Lleak*N3^2/N1^2];
Rg1=2.0;
Rg2=20;
Rg3=.005;
Rmat=[Rg1 0 0;0 Rg2 0; 0 0 -Rg3];
inv_Lmat = inv(Lmat);
Lmat2x2 = Lmat(2:3,2:3)
Rmat2x2 =Rmat(2:3,2:3)
inv_Lmat2x2 = inv(Lmat2x2);
```

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APPENDIX C

DuPont™ Kapton® PST

POLYIMIDE FILM

INDUSTRY SPECIFICATIONS
BULLETIN PST-00-1

Physical Properties of Kapton® 100 PST Film		
Physical Property	Typical value at	
	23°C	200°C
Ultimate Tensile Strength, MPa (psi)	252 (36,500)	139 (20,000)
Yield Point at 3%, MPa (psi)	69 (10,000)	41 (6,000)
Ultimate Elongation, %	72	93
Tensile Modulus, GPa (psi)	2.5 (370,000)	2.0 (290,000)
Tear Strength—Propagating (Elmendorf), N (lbf)	0.07 (0.02)	
Tear Strength—Initial (Graves), N (lbf)	7.2 (1.6)	

Introduction

These specifications include the values and tolerances for Kapton® PST film properties and the characteristics known to be of significance to coaters, laminators and manufacturers of pressure sensitive adhesive tape.

Any aspects of the specifications that require further interpretation or clarification should be discussed with representatives of DuPont High Performance Materials.

Kapton® PST Film

Kapton® PST is a tough film that exhibits an excellent balance of physical, chemical and electrical properties over a wide temperature range, particularly at unusually high temperatures. The film is available in 50, 100, 200, 300 and 500 gages.

Manufacturing

Material
Kapton® PST film is synthesized by a polycondensation reaction between an aromatic dianhydride and an aromatic diamine.

Uniformity
Material shall be uniform in composition, free of visual continuous surface scratches, and free of defects such as wrinkles, MD ridges, stretched lanes, holes, and particulate contamination that would prevent the user from producing acceptable quality products. The material will be processed in machines equipped with static eliminators to assure that the material will have less than 5,000 volts static charge. Roll telescoping will not exceed 1/16" (1.6 mm).

Cores
Roll cores shall be of sufficient strength to prevent collapsing from handling. The standard core internal diameters are nominally 3" and 6" (76 and 152 mm) with the following specifications:

3" I.D. =	3.032" ± 0.008" (77.01 ± 0.20 mm)
6" I.D. =	6.028" ± 0.015" (153.11 ± 0.40 mm)

The standard core material will be fiber. Other core material options, such as plastic, are available on request.

Width Tolerance

The maximum variation in film width from that specified on the order shall be as follows:

Slit Width Range	Tolerance
1" (25 mm) or less	±15 mil (±0.40 mm)
1 1/16" to 4" (27 to 102 mm)	±30 mil (±0.80 mm)
4 1/16" (103 mm) and wider	±60 mil (±1.50 mm)

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The miracles of science™

Length Tolerance

The nominal roll length is specified in **Table 1**. The actual measured roll length will be supplied on the core label of rolls that are 9" (229 mm) or wider. Lengths ordered in footage will be supplied to a tolerance of –0, +7% of footage ordered.

Pad Put-Ups

Available film widths and roll diameters are specified in **Table 1**. Larger put-ups of 6" x 18" (152 x 457 mm) are available on request.

Pad Roll Specifications

1. Core width will be the film width –0, +1/8" (3.2 mm)
2. Core edges shall not project more than 1/16" (1.6 mm) beyond the roll face on either side.
3. Core shall not be recessed on either side.
4. The outside and starting ends of the film shall be fastened in a manner to prevent unwinding.
5. "Dishing" or "cupping" may not exceed 1/16" (1.6 mm), measured with a straight edge across the diameter of the roll.

Table 1.

Type	Film thickness, mil (µm)	Width Range in (mm) Min.	Width Range in (mm) Max.	Size, I.D. x O.D. – in (mm) 3 x 6 (76 x 152)	3 x 9.5 (76 x 241)	6 x 9.5 (152 x 241)	6 x 11 (152 x 279)	6 x 14 (152 x 356)	Area Factor ft^2/lb (m^2/kg)
50PST	0.5 (13)	3/16 (5)	52 (1321)	3100 (945)	— 00	5900 (1769)	—	—	272 (55.6)
100PST	1.0 (25)	7/8 (22)	60 (1524)	—	5100 (1554)	—	5100 (1554)	—	136 (27.8)
200PST	2.0 (51)	7/8 (22)	60 (1524)	—	2550 (777)	—	2550 (777)	5000 (1524)	68 (13.9)
300PST	3.0 (76)	7/8 (22)	60 (1524)	—	1700 (518)	—	1700 (518)	3400 (1036)	45 (9.2)
500PST	5.0 (127)	7/8 (22)	60 (1524)	—	1000 (305)	—	1000 (305)	2020 (616)	27 (5.5)

Splices

Description

All film gauges are joined with a standard butt splice, with the butt edges covered on both sides with a Kapton® film based pressure sensitive adhesive tape. 2" wide splicing tape is used for all film gauges.

Splice Placement

Splice tape will be centered on the joint to ¼" (+6 mm). It will be smooth and wrinkle-free to avoid distortion of the adjacent film layers in the roll.

Table 2 shows the maximum number of splices per roll. It also shows the minimum length between splices and from the beginning and the end of a roll.

Table 2.

Core I.D. in (mm)	Roll O.D. in (mm)	Maximum Number of Splices per Roll 50PST	100PST	200PST	300PST	500PST	Minimum Length Between Splices or the Beginning and End of a Roll – ft (m) 50PST	100PST	200PST	300PST	500PST
3 (76)	6 (152)	5	—	—	—	—	100 (30)	—	—	—	—
6 (152)	9.5 (241)	10	—	—	—	—	100 (30)	—	—	—	—
3 (76)	9.5 (241)	—	6	4	3	3	—	100 (30)	100 (30)	100 (30)	75 (23)
6 (152)	11 (279)	—	6	4	3	3	—	100 (30)	100 (30)	100 (30)	75 (23)
6 (152)	14 (356)	—	10	7	5	5	—	100 (30)	100 (30)	100 (30)	75 (23)

Packaging and Marking

Packaging
Material shall be adequately packed to prevent loss of contents or damage during shipment. All film will be wrapped with a non-fibrous material.

Extra Core Label
An extra core label with the actual roll length shall be placed on the outside of the shipping container for roll widths of 9" (229 mm) and wider.

Marking
Material is identified as shown in **Table 3** to allow complete traceability to the raw materials and processing conditions:

Table 3. Package Marking

	Shipping Container	Package	Core Label*
Scheduled Date	x	x	x
Customer Order Number	x	x	x***
DuPont Order Number	x	x	x
Gauge	x	x	x
Type	x	x	x
Width	x	x	x
Number of Rolls per Container	x	x	
Net Weight	x	x	
Actual Footage			x
Batch Number	x	x	x
I.D. and O.D.**	x	x	

* Affixed to the core on all cores 2.25" (57 mm) wide and over. Included with the package on all cores less than 2.25" (57 mm) wide.
** Inside diameter of core and nominal outside diameter of roll.
*** Available for up to 12 characters.

Table 4. General Properties

Property	Film Type					Method
	50PST	100PST	200PST	300PST	500PST	
Average Thickness Unit Weight, gram/m²						Weigh test specimens equal to the width of slit roll and not less than 0.5 meters long to the nearest 0.10 gram on a torsion balance. To confirm average thickness tolerances, obtain a sample consisting of a minimum of one specimen from each of several randomly selected slit rolls as follows:
Minimum	14.0	33.0	68.1	102.1	169.5	
Maximum	26.0	35.0	74.2	115.2	192.5	
						Slit Roll Width / Under 6" (152 mm) / 6" (152 mm) and over — **Minimum No. of Slit Rolls to be Sampled** / 25 ÷ s.r width (in inches) / Four
Single Point Thickness, mil (µm)						Measure in accordance with ASTM D-374-79, Method A or C. Obtain the average of 10 randomly selected readings from a minimum area of 12 in² (77 cm²). Recheck before rejecting any slit roll. Abnormal readings may occasionally result from dust particles or spot surface imperfections. Discard such readings as they will adversely affect the accuracy of measurements designed to indicate general sheet thickness.
Minimum	0.35 (8.9)	0.90 (22.5)	1.85 (46.2)	2.72 (69.0)	4.65 (118.1)	
Maximum	0.65 (16.5)	1.05 (26.2)	2.15 (53.7)	3.28 (83.3)	5.35 (135.9)	

Table 5. Mechanical Properties

Property	Film Type					Method
	50PST	100PST	200PST	300PST	500PST	
Tensile Strength, psi (MPa), at 23°C. Machine Direction (MD) and Transverse Direction (TD) Minimum	26,000 (138)	30,000 (165)	30,000 (165)	30,000 (165)	30,000 (165)	ASTM D-882-91, Method A using an Instron Tensile Tester (specimen size: ½" x 6" [12.7 x 152 mm], jaw separation: 4" [102 mm], jaw speed: 2"/min [51 mm]). Calculate the average of 5 specimens based on original measured thickness.
Elongation, % MD and TD Minimum	50	60	60	65	65	Same as above.
Shrinkage, % MD and TD at 400°C Maximum	2.0	2.0	2.0	2.0	2.0	MIL-P-46112B (MR). The percent shrinkage is obtained for either the MD or TD by using the average of three measurements in either direction before and after conditioning. Prior to measurement the 8½" x 11" (216 x 279 mm) specimen is conditioned by freely suspending for 2 hr in an oven controlled to 400°C ± 2°C.
Moisture absorption, % Maximum	4.0	4.0	4.0	4.0	4.0	ASTM D-570-91, using 24 hr immersion at 23°C. Average of 3 specimens.

Table 6. Electrical Properties

Property	Film Type					Method
	50PST	100PST	200PST	300PST	500PST	
Dielectric Strength, AC volt/mil (kV/mm) Minimum	6,000 (119)	6,700 (236)	5,300 (197)	4,800 (177)	3,500 (119)	ASTM D-149-91. (Average of 10 specimens). Flat sheets in air placed between ½" (6 mm) diameter brass electrodes with 1/32" (0.8 mm) edge radius subjected to 60 cycles AC voltage at 500 volt/sec rate of rise to the breakdown voltage.
Volume Resistivity, Ω-cm at 200°C Minimum	10^{17}	10^{17}	10^{17}	10^{17}	10^{17}	ASTM D-257-78.
Dielectric Constant at 1 kHz Maximum	4.0	3.9	3.9	3.9	3.9	ASTM D-150-91. Use conducting silver paint electrodes, two terminal system of measurement at standard conditions. Results are based on an average of 5 tests using measured thickness of specimens.
Dissipation Factor at 1 kHz Maximum	0.0050	0.0036	0.0036	0.0036	0.0036	Same as above.

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K-10780 (11/05) Printed in the U.S.A.

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